AVR085: Replacing AT90S8515 by ATmega8515

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Introduction

This application note is a guide to assist current AT90S8515 users in converting existing designs to the ATmega8515. The ATmega8515 has two operating modes selected through the fuse settings. The S8515C Fuse selects whether the AT90S8515 compatibility mode should be used or not. By default, the S8515C Fuse is unprogrammed and the ATmega8515 does not operate in compatibility mode. When the compatibility mode is used, only non-conflicting enhancements make the part different from the AT90S8515. Additionally, the electrical characteristics of the ATmega8515 are different including an increase in operating frequency because of a change in process technology. Check the data sheet for detailed information. When the S8515C Fuse is unprogrammed, all new features are supported, but porting the code may require more work.

AT90S8515 Errata Corrected in ATmega8515

The following items from the Errata Sheets of the AT90S8515 do not apply to the ATmega8515. Refer to the AT90S8515 Errata Sheet for a more detailed description of the errata.

Note: Some of these errata entries were corrected in the last revision of AT90S8515. They are still referred, to ease converting from any AT90S8515 design.

LDS/STS when Accessing External RAM

LDS and STS do not corrupt any register in ATmega8515.

STS when Accessing the EEPROM

In ATmega8515, STS can be used to start an EEPROM write (EEWE in EECR) without any undesired behavior for the succeeding instruction.

8-bit AVR® Microcontroller

Application Note

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COM1B Settings Never Disconnects OC1B

In ATmega8515, Timer/Counter1 is disconnected from OC1B if COM1B1:0 = 0b00 in non-PWM mode, and when COM1B1:0 = 0b00 or 0b01 in PWM modes. In Normal mode, this means that the general port function takes control of the pin. In AT90S8515 compatibility mode, OC1B is low (but not tri-stated) when Timer/Counter1 is disconnected.

UART Looses Synchronization if RXD Line is Low when UART Receive is Disabled

The UART is replaced with a USART, which does not have this problem. The starting edge of a reception is only accepted as valid if the Receive Enable bit in the USART Control Register is set.

Releasing Reset Condition Without Clock

ATmega8515 has a new reset interface in which any external reset pulse exceeding the minimum pulse width t_{RST} causes an internal reset even though the condition disappears before any valid clock is present.

Lock Bits at High V_{CC}

There are no restrictions on the supply voltage or system frequency as long as the device is operated inside the voltage and frequency range prescribed in the data sheet for the ATmega8515.

SPI Can Send Wrong Byte

In ATmega8515, a new byte can be written to the SPI Data Register on the same clock edge as the previous transfer finishes. There is no need to wait for the previous transfer to complete before writing the next byte into the SPI Data Register when operating in Master mode.

Reset During EEPROM Write

If a Reset or Power-off occurs in ATmega8515 during an EEPROM write, the accessed location may be corrupted, but ATmega8515 will not corrupt any other locations than the one being written.

SPI Interrupt Flag Can be Undefined after Reset

ATmega8515 resets the SPI Interrupt Flag to zero.

Serial Programming at Voltages Below 3.0V

There are no restrictions on the supply voltage or system frequency as long as the device is operated inside the voltage and frequency range prescribed in the data sheet for the ATmega8515.

Skip Instruction with Interrupts

ATmega8515 interrupts always store the correct return address, also when interrupting a skip instruction skipping a two-word instruction.

Changes to Names

The following control bits have changed names, but have the same functionality and placement when accessed as in AT90S8515:

Table 1. Changed Bit Names

Bit Name in AT90S8515	Bit Name in ATmega8515	I/O Register (AT90S8515)	Comments
PWM10n	WGM1n0	TCCR1A	
PWM11	WGM11	TCCR1A	
CTC1	WGM12	TCCR1B	
WDTOE	WDCE	WDTCR	See “Changes to Watchdog Timer” on page 9.
CHR9	UCSZ2	UCR	
OR	DOR	USR	
SM	SM1	MCUCR	See “Improvements to Power Management” on page 6.

The following I/O Registers have changed names, but include the same functionality and placement when accessed as in AT90S8515:

Table 2. Changed Register Names

Register name in AT90S8515	Register name in ATmega8515	Comments
GIMSK	GICR	
MCUSR	MCUCSR	
UBRR	UBRRL	
USR	UCSRA	
UCR	UCSRB	

Improvements to Timer/Counters and Prescalers

For details about the improved and additional features, please refer to the data sheet. The following features have been added:

- The Prescalers in ATmega8515 can be Reset.
- Variable top value in PWM mode.
- For Timer/Counter1, Phase and Frequency Correct PWM mode in addition to the Phase Correct PWM mode.
- Fast PWM mode.
- Timer0 extended with PWM and Output Compare function.

Differences Between ATmega8515 and AT90S8515

Most of the improvements and changes apply to all the Timer/Counters and the description below is written in a general form. A lower case “x” replaces the output channel (A or B for Timer/Counter1, N/A for Timer/Counter0), while “n” replaces the Timer/Counter number (n = 0 or 1).

TCNT1 Cleared in PWM Mode

In AT90S8515 there are three different PWM resolutions – 8, 9, or 10 bits. Though only 8, 9, or 10 bits are compared, it is still possible to write values into the TCNT1 Register that exceed the resolution. Thus, the Timer/Counter has to complete the count to 0xFFFF before the reduced resolution becomes effective (i.e, if 8-bit resolution is selected and the TCNT1 Register contains 0x0100, the top value (0x00FF) will not be effective until the counter has counted up to 0xFFFF, turned, and counted down to 0x0000 again). In ATmega8515 this has been changed so that the unused bits in TCNT1 are being cleared to zero to avoid this unintended counting up to 0xFFFF. In the ATmega8515, the TCNT1 Register never exceeds the selected resolution.

ATmega8515

The most significant bits in the TCNT1 Register will be cleared at the first positive edge of the prescaled clock.

- 8-bit PWM: TCNT1H7:0 = 0
- 9-bit PWM: TCNT1H7:1 = 0
- 10-bit PWM: TCNT1H7:2 = 0

AT90S8515

TCNT1H not cleared.

OCR1xH Cleared in PWM Mode

Clearing OCR1xH in PWM mode is slightly different from clearing TCNT1. The AT90S8515 clears the six most significant bits if 8, 9, or 10 bits PWM mode is selected. Hence, if 0xFFFF is written to OCR1x in PWM-mode and OCR1x is read back, the result is 0x03FF regardless of which PWM mode that is selected. In ATmega8515 the number of cleared bits depends on the resolution.

ATmega8515

The most significant bits in OCR1AH and OCR1BH are cleared when they are updated at the TOP-value of the counter.

- 8-bit PWM: OCR1xH7:0 = 0
- 9-bit PWM: OCR1xH7:1 = 0
- 10-bit PWM: OCR1xH7:2 = 0

AT90S8515

The six most significant bits in the OCR1AH and OCR1BH are cleared regardless of the resolution.

Clear Timer/Counter1 on Compare Match with Prescaler

The relation between a Clear on Compare Match and the internal counting of the Timer/Counter1 has been changed. The Clear on Compare Match in the AT90S8515 clears the Timer/Counter1 after the first internal count matching the compare value, whereas the ATmega8515 clears Timer/Counter1 after the last internal count matching the compare value. See Figure 1 and Figure 2 for details on clearing, flag setting, and pin change.

Example: OCR1x = 0x02 when prescaler is enabled (divide clock by 8).

Figure 1. Setting Output Compare Flag/Pin for AT90S8515[1]

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 0 0 0 0 0 0 0
Pin/Flag	h h

Note: 1. "h" Indicates where the Output Compare Flag/Pin will be set.

Figure 2. Setting Output Compare Flag/Pin for ATmega8515[1]

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1
Pin/Flag	h

Note: 1. "h" Indicates where the Output Compare Flag/Pin will be set.

Setting of Output Compare Pin/Flag with Prescaler Enabled

The relation between an Output Compare and the internal counting of the Timer/Counter1 has been changed. Output Compare in the AT90S8515 sets the Output Compare pin/flag after the first internal count matching the compare value, whereas the ATmega8515 sets the Output Compare pin/flag after the last internal count matching the compare value. See Figure 3 and Figure 4 for details on Output Compare Flag setting and pin change.

Example: OCR1x = 0x02, prescaler enabled (divide clock by 8).

Figure 3. Setting Output Compare Flag/Pin for AT90S8515[1]

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4
Pin/Flag	h

Note: 1. "h" Indicates where the Output Compare Flag/Pin will be set.

Figure 4. Setting Output Compare Flag/Pin for ATmega8515[1]

TCNTn	0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 2 2 2 2 2 2 2 2 3 3 3 3 3 3 3 3 4 4 4 4 4 4 4 4
Pin/Flag	h

Note: 1. "h" Indicates where the Output Compare Flag/Pin will be set.

Write to OCR1x in PWM Mode, Change to Normal Mode Before OCR1x is Updated at the Top, Read OCR1x

As described in the data sheet, the OCR1x Registers are updated at the top value when written. Thus, when writing the OCR1x in PWM mode, the value is stored in a temporary buffer. When the Timer/Counter reaches the top, the temporary buffer is transferred to the actual Output Compare Register. If PWM mode is left after the temporary buffer is written, but before the actual Output Compare register is updated, the behavior differs between ATmega8515 and AT90S8515.

ATmega8515

If the OCR1x Register is read before the update is done, the actual compare value is read – not the temporary OCR1x buffer.

AT90S8515

If the OCR1x Register is read before the update is done, the value in the OCR1x buffer is read. For example, the value read is the one last written (to the OCR1x buffer), but since the Timer/Counter never reached the top value, it was not latched into the OCR1x Register. Hence, the value that is used for comparison is not necessarily the same as being read.

Memory of Previous OCnx Pin Level

In AT90S8515, there are two settings of COMnx1:0 that do not update the OCnx pin in PWM mode (0b00 and 0b01), and one setting of COMnx1:0 in non-PWM mode (0b00). Assume the Timer/Counter is taken from a state that updates the OCnx pin to a state that does not, and then back again to a state that does update the OCnx pin. The following differences should be noted:

ATmega8515

The level of the OCnx pin before disabling the Output Compare mode is remembered. Re-enabling the Output Compare mode will cause the OCnx pin to resume operation from the state it had when it was disabled. All Output Compare pins are initialized to zero on reset.

AT90S8515

For Timer/Counter1 in non-PWM mode, a compare match during the time when the Timer/Counter is not connected to the pin will reset the OCnx pin to the low level once enabled again. PWM mode will update the internal register for the OCnx pin, such that the state of the pin is unknown once enabled again.

Improvements to External Memory Interface

The combined Address/Data port in ATmega8515 outputs data until a new address is set up. Refer to the ATmega8515 data sheet for details on the changed timing.

Improvements to Power Management

ATmega8515 contains more sleep modes than AT90S8515. This means that the SM bit in AT90S8515 is extended to SM2:0 in ATmega8515. SM = “0” in AT90S8515 corresponds to SM2:0 = 0b000 in ATmega8515, and SM = “1” in AT90S8515 corresponds to SM2:0 = 0b010 in ATmega8515. However, the bit position for SM in AT90S8515 equals the bit position for SM1 in ATmega8515. This means that ATmega8515 is fully backward compatible to AT90S8515 without any modification to the code regarding power management.

See data sheet for ATmega8515 for a description of the additional sleep modes.

Improvements to SPI and UART

Both SPI and USART have new Double Speed modes which allow higher communication speed.

The UART in AT90S8515 has been replaced by a USART in ATmega8515. The ATmega8515 USART is compatible with the AT90S8515 UART with one exception: The two-level Receive Register acts as a FIFO. The FIFO is disabled when the S8515C Fuse is programmed. Still the following must be kept in mind when the S8515C Fuse is programmed:

- The UDR must only be read once for each incoming data.
- The Error Flags (FE and DOR) and the ninth data bit (RXB8) are buffered with the data in the receive buffer. Therefore the status bits must always be read before the UDR Register is read. Otherwise, the error status will be lost.

Another minor difference is the initial value of RXB8, which is “1” in the UART in AT90S8515 and “0” in the USART in ATmega8515

Changes to EEPROM Write Timing

In AT90S8515, the EEPROM write time is dependent on supply voltage, typically 2.5 ms @ V_{CC} = 5V and 4 ms @ V_{CC} = 2.7V. In ATmega8515, the EEPROM write time takes 8,448 cycles of the calibrated RC Oscillator (regardless of the clock source and frequency for the system clock). The calibrated RC Oscillator is assumed to be calibrated to 1.0 MHz regardless of V_{CC}, i.e., typical write time is 8.4 ms.

Note: Changing the value in the OSCCAL Register affects the frequency of the calibrated RC Oscillator and hence the EEPROM write time.

Programming Interface

Some changes have been done to the programming interface, especially in the In-System Programming interface. This has been done to support all the additional fuses in ATmega8515. The timing requirements are unchanged. See the ATmega8515 data sheet for details.

The Parallel Programming algorithm is changed. The most significant change is the introduction of the PAGEL pin on PD7, and the BS2 pin on PA0. This extension is needed to support page programming of Flash, EEPROM and additional fuses in ATmega8515. Note that the additional fuses and Lock bits also require a change in the fuse writing algorithm. The timing requirements for Parallel programming have been changed. See the ATmega8515 data sheet for details.

The STK500 supports both In-System Programming and Parallel Programming of the ATmega8515.

Fuse Settings

ATmega8515 contains more fuses than AT90S8515. Table 3 shows the AT90S8515 compatible Fuse settings. Some of the fuses are described further in the following sections.

Table 3. Comparing Fuses in AT90S8515 and ATmega8515[1]

Fuse	Default AT90S8515 Setting	Default ATmega8515 Setting	AT90S8515 Compatible Setting
S8515C	–	1	0
WDTON	–	1	1
SPIEN	0	0	0
CKOPT	–	1	0[2]
EESAVE	–	1	1
BOOTSZ1	–	0	0 (N/A)[3]
BOOTSZ0	–	0	0 (N/A)[3]
BOOTRST	–	1	1
BODLEVEL	–	1	1
BODEN	–	1	1
SUT1	–	1	See note [4]
SUT0	–	0	See note [4]
CKSEL3	–	0	See note [4]
CKSEL2	–	0	See note [4]
CKSEL1	–	0	See note [4]
CKSEL0	–	1	See note [4]

Notes:
1. A dash indicates that the fuse is not present in AT90S8515.
2. See “Oscillators and Selecting Start-up Delays” on page 8.
3. SPM and Self-Programming is not available in AT90S8515. The default factory setting of BOOTSZ1:0 is OK when porting the design to ATmega8515.
4. The SUT Fuses in ATmega8515 replaces the FSTRT Fuse in AT90S8515. The SUT and CKSEL setting must be considered when moving to ATmega8515. See “Oscillators and Selecting Start-up Delays” on page 8.

Oscillators and Selecting Start-up Delays

ATmega8515 provides more Oscillators and Start-up time selections than AT90S8515. During wake-up from Power-down mode, the ATmega8515 uses the CPU frequency to determine the duration of the wake-up delay, while AT90S8515 determines the delay from the WDT Oscillator frequency.

Follow the guidelines from the section “System Clock and Clock Options” in the ATmega8515 data sheet to find appropriate start-up values.

Special attention must be paid when changing the fuses in In-System Programming mode. In-System Programming is dependent on a system clock. If wrong Oscillator setting is programmed, it may be impossible to re-enter In-System Programming mode due to missing system clock (Parallel Programming mode must then be used).

The crystal Oscillator in AT90S8515 is capable of driving an addition clock buffer from the XTAL2 output. In ATmega8515, this is only possible when the CKOPT Fuse is programmed. In this mode the Oscillator has a rail-to-rail swing at the output, but at the

expense of higher power consumption. Hence, do only program this fuse when rail-to-rail swing is required.

Changes to Watchdog Timer

The Watchdog Timer in ATmega8515 is improved compared to the one in AT90S8515. In AT90S8515, the Watchdog Timer is either enabled or disabled, while ATmega8515 supports two safety levels selected by the WDTON Fuse. See description in ATmega8515 data sheet for further information.

The combination of programming the S8515C Fuse and having the WDTON Fuse unprogrammed makes the Watchdog Timer behave exactly as in AT90S8515.

The frequency of the Watchdog Oscillator in ATmega8515 is close to 1.0 MHz for all supply voltages. The typical frequency of the Watchdog Oscillator in AT90S8515 is close to 1.0 MHz at 5V, but the Time-out period increases with decreasing V_{CC}. This means that the selection of Time-out period for the Watchdog Timer (in terms of number of WDT Oscillator cycles) must be reconsidered when porting the design to ATmega8515. Refer to the data sheet for ATmega8515 for further information.

Other Concerns

The ATmega8515 has a signature byte different from the one used in AT90S8515. Make sure you are using the signature byte of ATmega8515 when porting the design.

Features not Available in AT90S8515 Compatibility Mode

The S8515C Fuse makes the ATmega8515 compatible to AT90S8515. However, with the S8515C Fuse programmed, some of the new features in ATmega8515 become unavailable. The following features are not supported when the ATmega8515 is used in the AT90S8515 compatibility mode:

- The FIFO operation of the USART.
- A timed sequence to change Watchdog Timer prescaler settings by software.
- Port E (Dedicated functions only in AT90S8515 compatibility mode).

If any of the features above are needed or wanted and the S8515C Fuse is unprogrammed, this introduces some differences between ATmega8515 and AT90S8515 which do not exist as long as the compatibility fuse is programmed:

- Port E is not initialized upon reset to drive 0 at PE1 and PE2, but it is tri-stated as all other ports.
- A timed sequence must be followed to change Watchdog Timer prescaler settings by software.
- The UART will have an extra input buffer which allows one more data byte to be received before the Data OverRun Flag (DOR) is set.

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