8-Bit AVR® Microcontroller with 2K Bytes of In-System Programmable Flash

AT90S2323 AT90LS2323 AT90S2343 AT90LS2343 Preliminary

Features

- **Utilizes the *AVR*® Enhanced RISC Architecture**
- ***AVR* - High Performance and Low Power RISC Architecture**
- **118 Powerful Instructions - Most Single Clock Cycle Execution**
- **2K bytes of In-System Programmable ISP Flash**
  - **SPI Serial Interface for In-System Programming**
  - **Endurance: 1,000 Write/Erase Cycles**
- **128 bytes EEPROM**
  - **Endurance: 100,000 Write/Erase Cycles**
- **128 bytes Internal RAM**
- **32 x 8 General Purpose Working Registers**
  - **3 AT90S/LS2323 Programmable I/O Lines**
  - **5 AT90S/LS2343 Programmable I/O Lines**
- **V_{CC}: 4.0 - 6.0V AT90S2323/AT90S2343**
- **V_{CC}: 2.7 - 6.0V AT90LS2323/AT90LS2343**
- **Power-On Reset Circuit**
- **Speed Grades: 0 - 10 MHz AT90S2323/AT90S2343**
- **Speed Grades: 0 - 4 MHz AT90LS2323/AT90LS2343**
- **Up to 10 MIPS Throughput at 10 MHz**
- **One 8-Bit Timer/Counter with Separate Prescaler**
- **External and Internal Interrupt Sources**
- **Programmable Watchdog Timer with On-Chip Oscillator**
- **Low Power Idle and Power Down Modes**
- **Programming Lock for Flash Program and EEPROM Data Security**
- **Selectable On-Chip RC Oscillator**
- **8-Pin Device**

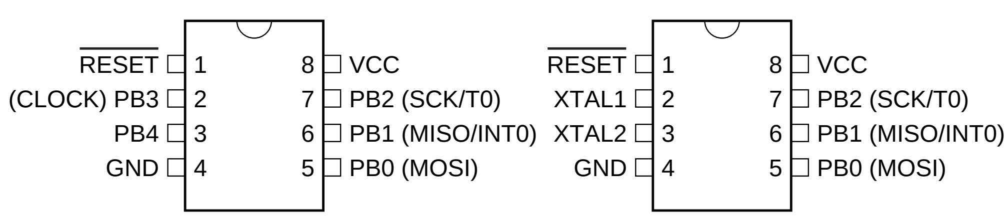
Description

The AT90S/LS2323 and AT90S/LS2343 is a low-power CMOS 8-bit microcontrollers based on the *AVR*® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the AT90S/LS2323 and AT90S/LS2343 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

Pin Configuration

PDIP/SOIC



AT90S/LS2343 AT90S/LS2323

Rev. 1004A–05/98

Block Diagram

Figure 1. The AT90S/LS2343 Block Diagram

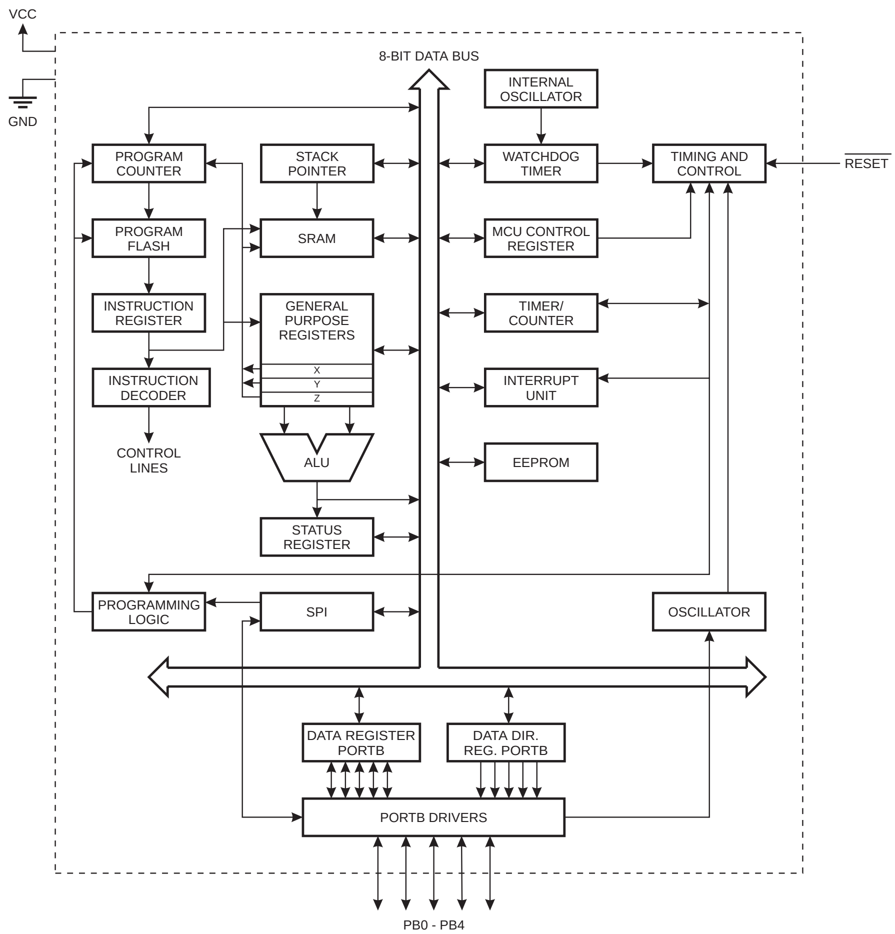
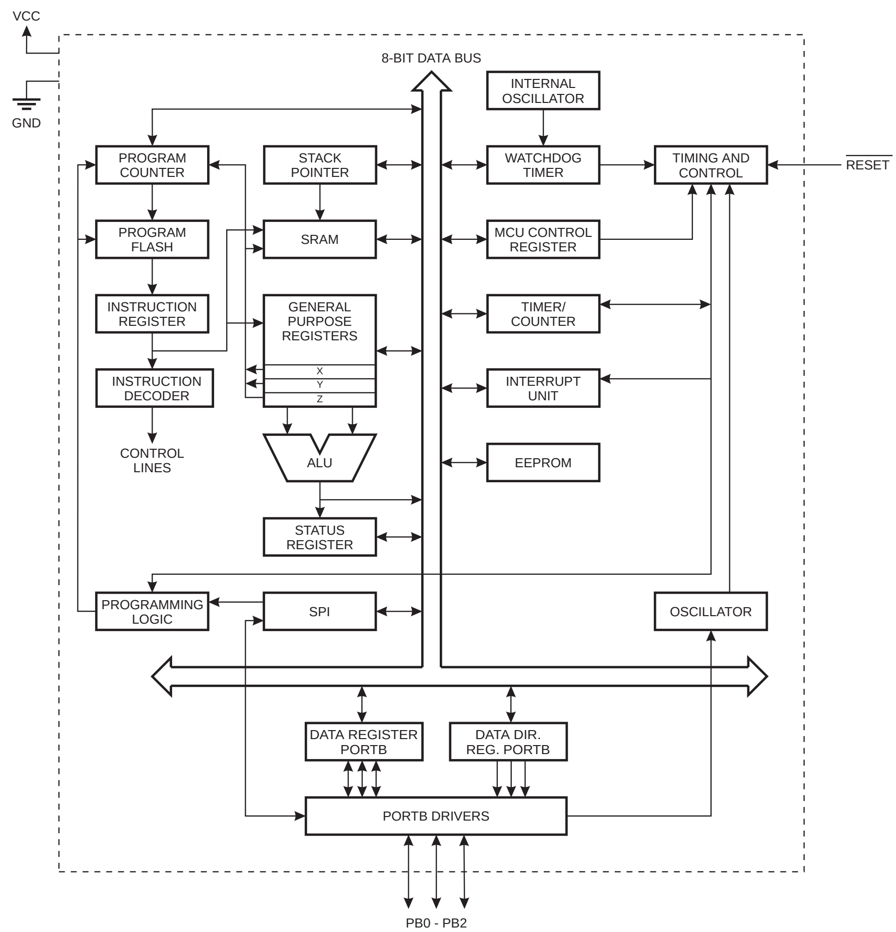


Figure 2. The AT90S/LS2323 Block Diagram



Description

The AT90S/LS2323 and AT90S/LS2343 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 3 (AT90S/LS2323) / 5 (AT90S/LS2343) general purpose I/O lines, 32 general purpose working registers, an 8-bit timer/counter, internal and external interrupts, programmable Watchdog Timer with internal oscillator, an SPI serial port for Flash Memory downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high density non-volatile memory technology. The on-chip Flash allows the program memory to be reprogrammed in-system through an SPI serial interface. By combining an 8-bit RISC CPU with ISP Flash on a monolithic chip, the Atmel AT90S/LS2323 and AT90S/LS2343 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The AT90S/LS2323 and AT90S/LS2343 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

Comparison Between AT90S/LS2323 and AT90S/LS2343

The AT90S/LS2323 is intended for use with external quartz crystal or ceramic resonator as the clock source. The start-up time is fuse selectable as either 1 ms (suitable for ceramic resonator) or 16 ms (suitable for crystal). The device has three I/0 pins.

The AT90S/LS2343 is intended for use with either an external clock source or the internal RC oscillator as clock source. The device has five I/0 pins.

Table 1 summarizes the differences in features of the two devices.

Table 1. Feature Difference Summary

Part	AT90S/LS2323	AT90S/LS2343
On-chip oscillator amplifier	yes	no
Internal RC Clock	no	yes
PB3 usable	never	internal clock mode
PB4 usable	never	always
Startup time	1 ms / 16 ms	16 µs fixed

Pin Descriptions AT90S/LS2323

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB2..PB0)

Port B is a 3-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit).

$\overline{\text{RESET}}$

Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Pin Descriptions AT90S/LS2343

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB4..PB0)

Port B is a 5-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). When the device is clocked from an external clock source, PB3 is used as the clock input.

$\overline{\text{RESET}}$

Reset input. A low on this pin for two machine cycles while the oscillator is running resets the device.

CLOCK

Clock signal input in external clock mode.

Clock Sources

The AT90S/LS2323 contains an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 3. XTAL1 and XTAL2 are input and output respectively. Either a quartz crystal or a ceramic resonator may be used. It is recommended to use the AT90S/LS2343 if an external clock source is used, since this gives an extra I/O pin.

The AT90S/LS2343 can be clocked by an external clock signal, as shown in Figure 4, or by the on-chip RC oscillator. This RC oscillator runs at a nominal frequency of 1 MHz (VCC = 5V). A fuse bit - RCEN - in the Flash memory selects the on-chip RC oscillator as the clock source when programmed ('0'). The AT90S/LS2343 is shipped with this bit programmed.

Figure 3. Oscillator Connection

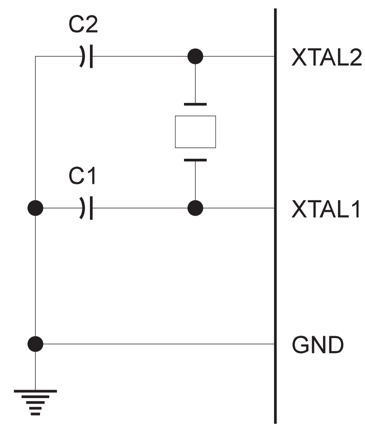
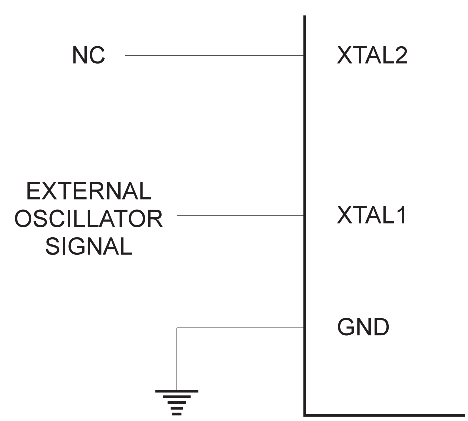


Figure 4. External Clock Drive Configuration



AT90S/LS2323 and AT90S/LS2343 Architectural Overview

The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file - in one clock cycle.

Six of the 32 registers can be used as three 16-bits indirect address register pointers for Data Space addressing-enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bit X-register, Y-register and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 5 shows the AT90S/LS2323 and AT90S/LS2343 *AVR* Enhanced RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses ($00 - $1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O memory can be accessed directly, or as the Data Space locations following those of the register file, $20 - $5F.

The *AVR* has Harvard architecture - with separate memories and buses for program and data. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system downloadable Flash memory.

With the relative jump and call instructions, the whole 1K address space is directly accessed. Most *AVR* instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

The 128 bytes data SRAM + register file and I/O registers can be easily accessed through the five different addressing modes supported in the *AVR* architecture.

The memory spaces in the *AVR* architecture are all linear and regular memory maps.

Figure 5. The AT90S/LS2323 and AT90S/LS2343 AVR Enhanced RISC Architecture

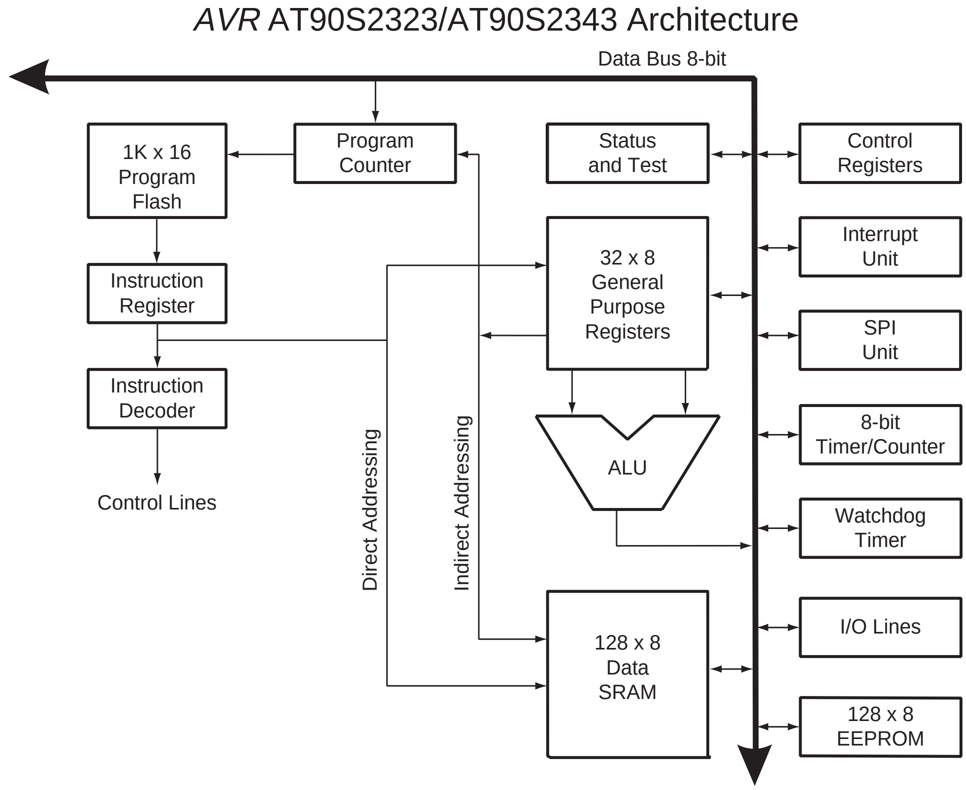
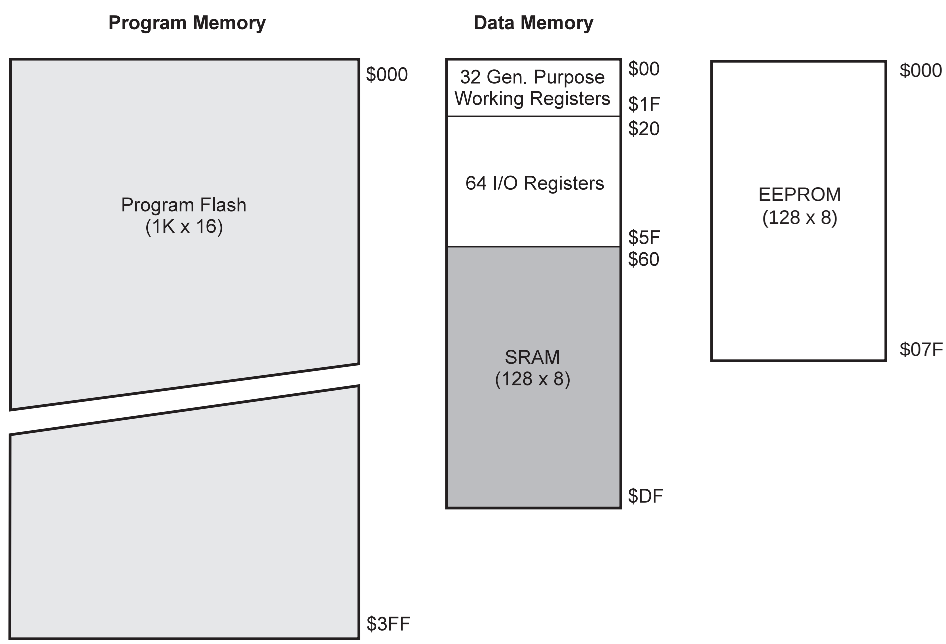


Figure 6. Memory Maps



A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

The General Purpose Register File

Figure 7 shows the structure of the 32 general purpose registers in the CPU.

Figure 7. *AVR* CPU General Purpose Working Registers

	7 0	Addr.	
	R0	$00	
	R1	$01	
	R2	$02	
	…		
	R13	$0D	
General	R14	$0E	
Purpose	R15	$0F	
Working	R16	$10	
Registers	R17	$11	
	…		
	R26	$1A	X-register low byte
	R27	$1B	X-register high byte
	R28	$1C	Y-register low byte
	R29	$1D	Y-register high byte
	R30	$1E	Z-register low byte
	R31	$1F	Z-register high byte

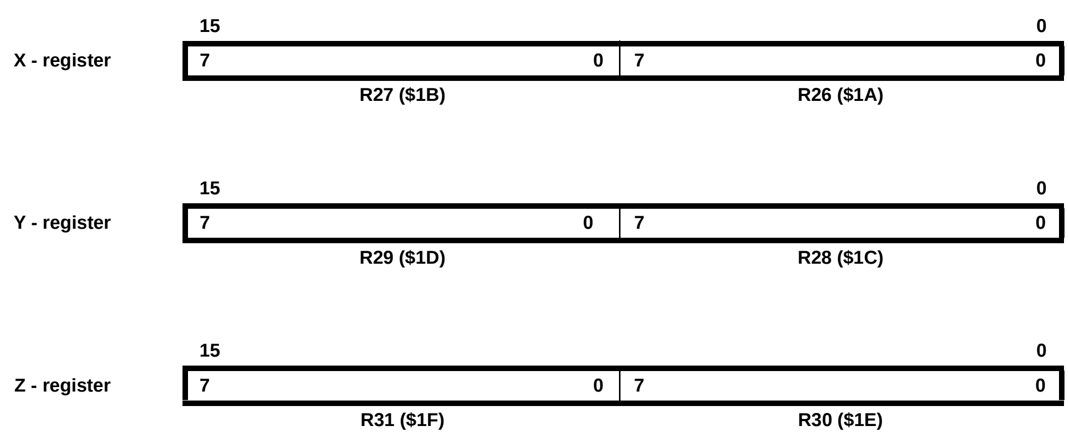
All the register operating instructions in the instruction set have direct and single cycle access to all registers. The only exception is the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, ORI between a constant and a register and the LDI instruction for load immediate constant data. These instructions apply to the second half of the registers in the register file - R16..R31. The general SBC, SUB, CP, AND, OR and all other operations between two registers or on a single register apply to the entire register file.

As shown in Figure 7, each register is also assigned a data memory address, mapping them directly into the first 32 locations of the user Data Space. Although the register file is not physically implemented as SRAM locations, this memory organization provides great flexibility in access of the registers, as the X, Y and Z registers can be set to index any register in the file.

The X-Register, Y-Register, and Z-Register

The registers R26..R31 have some added functions to their general purpose usage. These registers are the address pointers for indirect addressing of the Data Space. The three indirect address registers X, Y and Z are defined as:

Figure 8. The X, Y, and Z Registers



In the different addressing modes these address registers have functions as fixed displacement, automatic increment and decrement (see the descriptions for the different instructions).

The ALU - Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories - arithmetic, logic and bit-functions

The In-System Programmable Flash Program Memory

The AT90S/LS2323 and AT90S/LS2343 contains 2K bytes on-chip In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 1K x 16. The Flash memory has an endurance of at least 1000 write/erase cycles.

The AT90S/LS2323 and AT90S/LS2343 Program Counter PC is 10 bits wide, hence addressing the 1024 program memory addresses.

See page 25 for a detailed description on Flash data programming.

Constant tables must be allocated within the address 0-2K (see the LPM - Load Program Memory instruction description).

See page 8 for the different addressing modes.

The EEPROM Data Memory

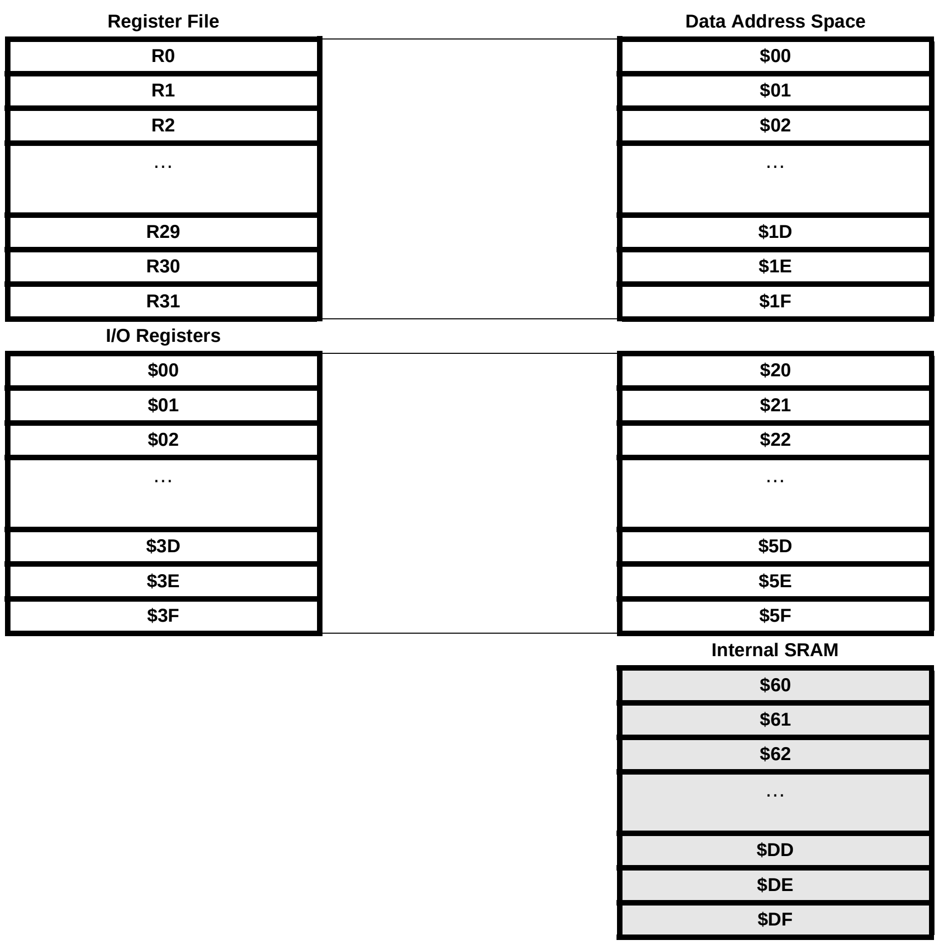
The AT90S/LS2323 and AT90S/LS2343 contains 128 bytes of EEPROM data memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 100,000 write/erase cycles. The access between the EEPROM and the CPU is described on page 21 specifying the EEPROM address register, the EEPROM data register, and the EEPROM control register.

For the SPI data downloading, see page 25 for a detailed description.

The SRAM Data Memory

The following figure shows how the AT90S/LS2323 and AT90S/LS2343 Data Memory is organized:

Figure 9. SRAM Organization



The 224 Data Memory locations address the Register file, I/O Memory and the data SRAM. The first 96 locations address the Register File + I/O Memory, and the next 128 locations address the data SRAM.

The five different addressing modes for the data memory cover: Direct, Indirect with Displacement, Indirect, Indirect with Pre-Decrement and Indirect with Post-Increment. In the register file, registers R26 to R31 feature the indirect addressing pointer registers.

The Direct addressing reaches the entire data address space.

The Indirect with Displacement mode features 63 address locations reach from the base address given by the Y and Z register.

When using register indirect addressing modes with automatic pre-decrement and post-increment, the address registers X, Y and Z are used and decremented and incremented.

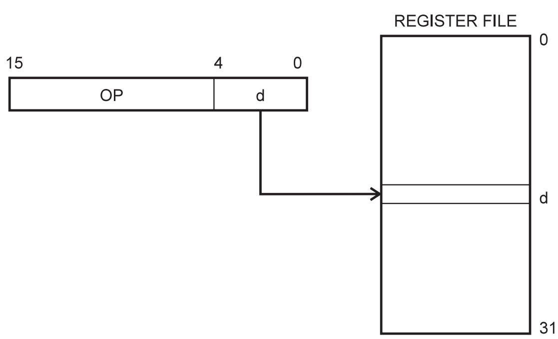
The 32 general purpose working registers, 64 I/O registers and the 128 bytes of data SRAM in the AT90S/LS2323 and AT90S/LS2343 are all directly accessible through all these addressing modes.

The Program and Data Addressing Modes

The AT90S/LS2323 and AT90S/LS2343 AVR Enhanced RISC Microcontroller supports powerful and efficient addressing modes for access to the program memory (Flash) and data memory. This section describes the different addressing modes supported by the AVR architecture. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single Register Rd

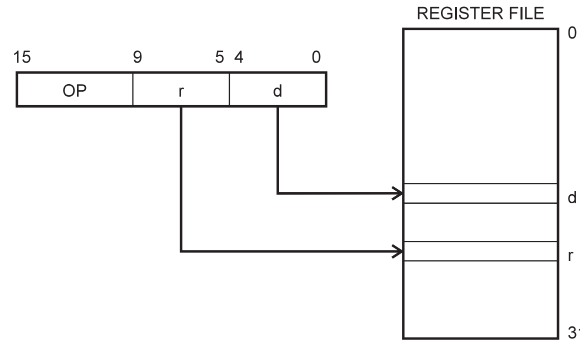
Figure 10. Direct Single Register Addressing



The operand is contained in register d (Rd).

Register Direct, Two Registers Rd and Rrv

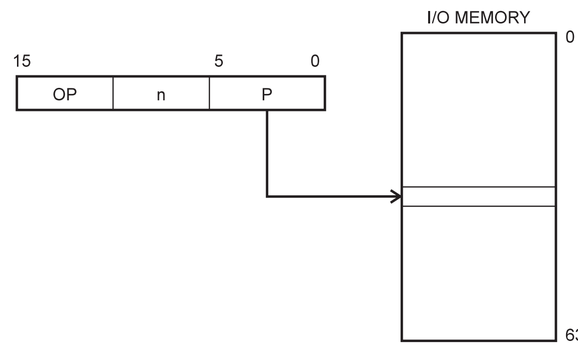
Figure 11. Direct Register Addressing, Two Registers



Operands are contained in register r (Rr) and d (Rd). The result is stored in register d (Rd).

I/O Direct

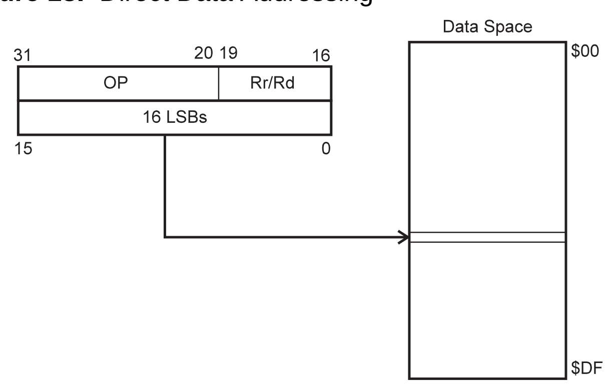
Figure 12. I/O Direct Addressing



Operand address is contained in 6 bits of the instruction word. n is the destination or source register address.

Data Direct

Figure 13. Direct Data Addressing



A 16-bit Data Address is contained in the 16 LSBs of a two-word instruction. Rd/Rr specify the destination or source register.

Data Indirect with Displacement

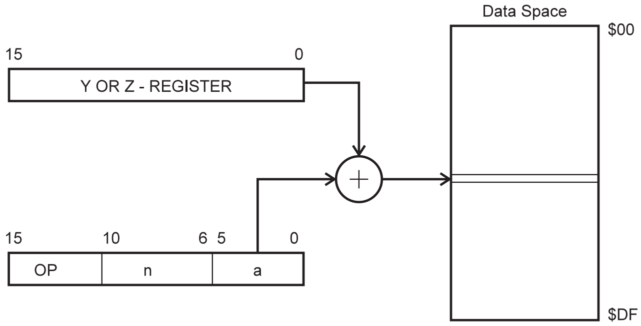


Figure 14. Data Indirect with Displacement

Operand address is the result of the Y or Z-register contents added to the address contained in 6 bits of the instruction word.

Data Indirect

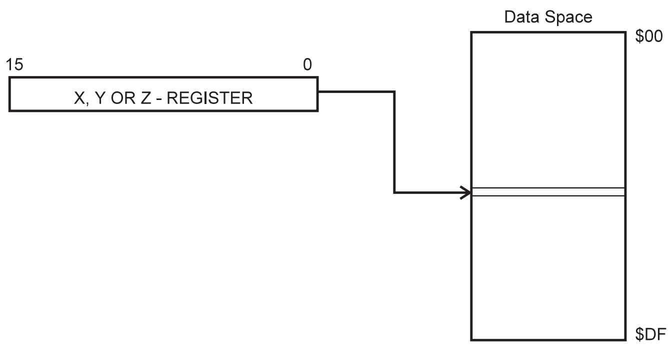


Figure 15. Data Indirect Addressing

Operand address is the contents of the X, Y or the Z-register.

Data Indirect With Pre-Decrement

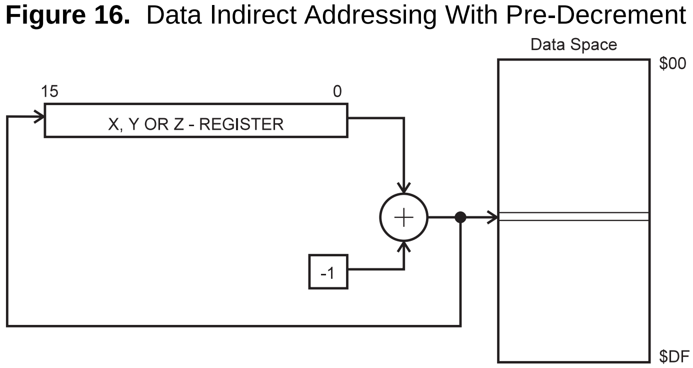


Figure 16. Data Indirect Addressing With Pre-Decrement

The X, Y or the Z-register is decremented before the operation. Operand address is the decremented contents of the X, Y or the Z-register.

Data Indirect With Post-Increment

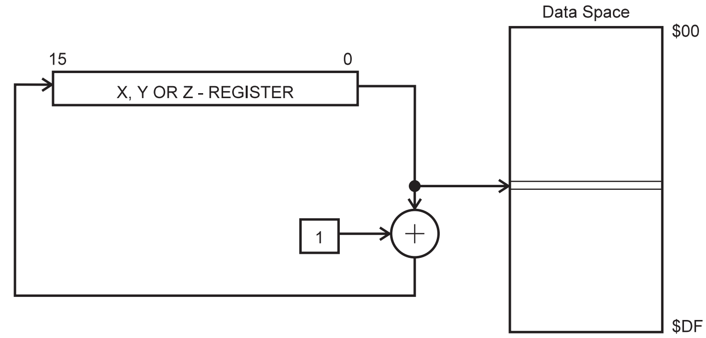


Figure 17. Data Indirect Addressing With Post-Increment

The X, Y or the Z-register is incremented after the operation. Operand address is the content of the X, Y or the Z-register prior to incrementing.

Constant Addressing Using the LPM Instruction

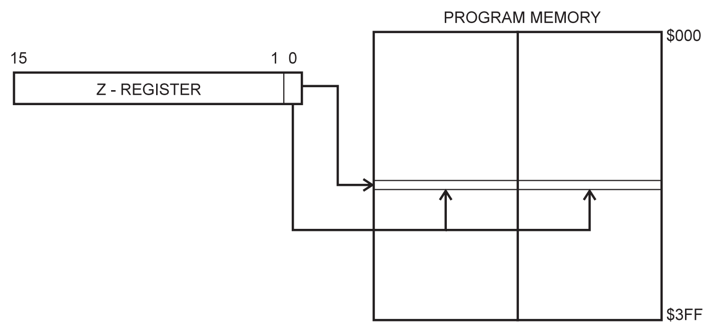


Figure 18. Code Memory Constant Addressing

Constant byte address is specified by the Z-register contents. The 15 MSBs select word address (0 - 1K), and LSB selects low byte if cleared (LSB = 0) or high byte if set (LSB = 1).

Indirect Program Addressing, IJMP and ICALL

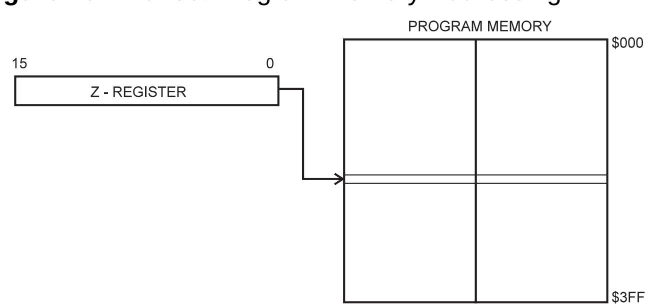
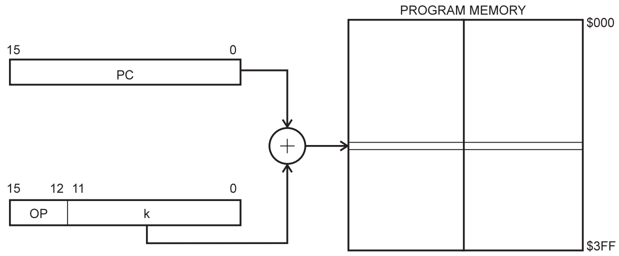


Figure 19. Indirect Program Memory Addressing

Program execution continues at address contained by the Z-register (i.e., the PC is loaded with the content of the Z-register).

Relative Program Addressing, RJMP and RCALL

Figure 20. Relative Program Memory Addressing



Program execution continues at address PC + k + 1. The relative address k is -2048 to 2047.

Memory Access and Instruction Execution Timing

This section describes the general access timing concepts for instruction execution and internal memory access.

The *AVR* CPU is driven by the System Clock Ø, directly generated from the external clock signal applied to the CLOCK pin. No internal clock division is used.

Figure 21. The Parallel Instruction Fetches and Instruction Executions

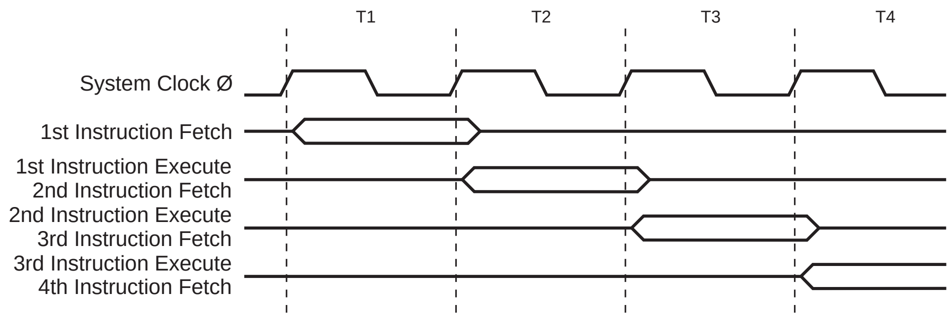


Figure 21 shows the parallel instruction fetches and instruction executions enabled by the Harvard architecture and the fast-access register file concept. This is the basic pipelining concept to obtain up to 1 MIPS per MHz with the corresponding unique results for functions per cost, functions per clocks, and functions per power-unit.

Figure 22. Single Cycle ALU Operation

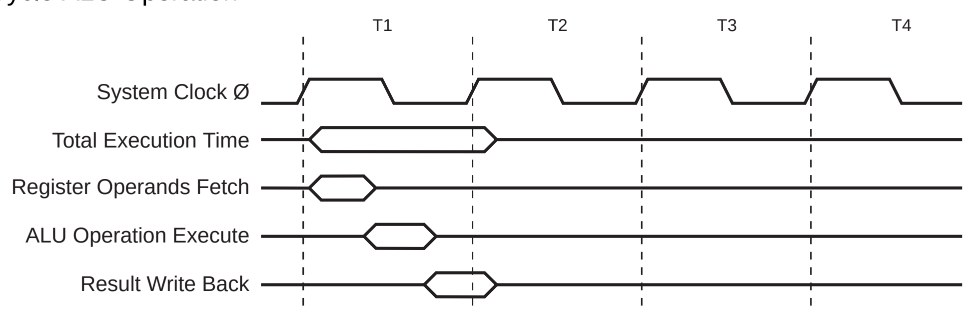
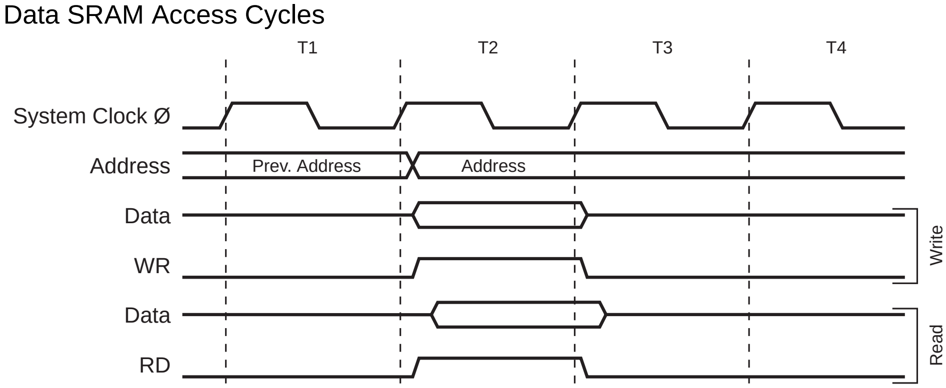


Figure 22 shows the internal timing concept for the register file. In a single clock cycle an ALU operation using two register operands is executed, and the result is stored back to the destination register.

Figure 23. On-Chip Data SRAM Access Cycles



The internal data SRAM access is performed in two System Clock cycles as described in Figure 23.

I/O Memory

The I/O space definition of the AT90S/LS2323 and AT90S/LS2343 is shown in the following table:

Table 1. AT90S/LS2323 and AT90S/LS2343 I/O Space

Address Hex	Name	Function
$3F ($5F)	SREG	Status REGister
$3D ($5D)	SPL	Stack Pointer Low
$3B ($5B)	GIMSK	General Interrupt MaSK register
$3A ($5A)	GIFR	General Interrupt Flag Register
$39 ($59)	TIMSK	Timer/Counter Interrupt MaSK register
$38 ($58)	TIFR	Timer/Counter Interrupt Flag register
$35 ($55)	MCUCR	MCU Control Register
$34 ($54)	MCUSR	MCU Status Register
$33 ($53)	TCCR0	Timer/Counter 0 Control Register
$32 ($52)	TCNT0	Timer/Counter 0 (8-bit)
$21 ($41)	WDTCR	Watchdog Timer Control Register
$1E ($3E)	EEAR	EEPROM Address Register
$1D ($3D)	EEDR	EEPROM Data Register
$1C ($3C)	EECR	EEPROM Control Register
$18 ($38)	PORTB	Data Register, Port B
$17 ($37)	DDRB	Data Direction Register, Port B
$16 ($36)	PINB	Input Pins, Port B

Note: Reserved and unused locations are not shown in the table.

All the different AT90S/LS2323 and AT90S/LS2343 I/O and peripherals are placed in the I/O space. The different I/O locations are accessed by the IN and OUT instructions transferring data between the 32 general purpose working registers and the I/O space. I/O registers within the address range $00 - $1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions. Refer to the instruction set chapter for more details.

When using the I/O specific commands, IN, OUT, SBIS and SBIC, the I/O addresses $00 - $3F must be used. When addressing I/O registers as SRAM, $20 must be added to this address. All I/O register addresses throughout this document are shown with the SRAM address in parentheses.

The different I/O and peripherals control registers are explained in the following sections.

The Status Register - SREG

The AVR status register - SREG - at I/O space location $3F ($5F) is defined as:

Bit	7	6	5	4	3	2	1	0	
$3F ($5F)	I	T	H	S	V	N	Z	C	SREG
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - I: Global Interrupt Enable**

The global interrupt enable bit must be set (one) for the interrupts to be enabled. The individual interrupt enable control is then performed in the interrupt mask registers - GIMSK and TIMSK. If the global interrupt enable register is cleared (zero), none of the interrupts are enabled independent of the GIMSK and TIMSK values. The I-bit is cleared by hardware after an interrupt has occurred, and is set by the RETI instruction to enable subsequent interrupts.

- **Bit 6 - T: Bit Copy Storage**

The bit copy instructions BLD (Bit LoaD) and BST (Bit STore) use the T bit as source and destination for the operated bit. A bit from a register in the register file can be copied into T by the BST instruction, and a bit in T can be copied into a bit in a register in the register file by the BLD instruction.

- **Bit 5 - H: Half Carry Flag**

The half carry flag H indicates a half carry in some arithmetic operations. See the Instruction Set Description for detailed information.

- **Bit 4 - S: Sign Bit, S = N ⊕ V**

The S-bit is always an exclusive or between the negative flag N and the two's complement overflow flag V. See the Instruction Set Description for detailed information.

- **Bit 3 - V: Two's Complement Overflow Flag**

The two's complement overflow flag V supports two's complement arithmetics. See the Instruction Set Description for detailed information.

- **Bit 2 - N: Negative Flag**

The negative flag N indicates a negative result after the different arithmetic and logic operations. See the Instruction Set Description for detailed information.

- **Bit 1 - Z: Zero Flag**

The zero flag Z indicates a zero result after the different arithmetic and logic operations. See the Instruction Set Description for detailed information.

- **Bit 0 - C: Carry Flag**

The carry flag C indicates a carry in an arithmetic or logic operation. See the Instruction Set Description for detailed information.

The Stack Pointer - SPL

An 8-bit register at I/O address $3D ($5D) forms the stack pointer of the AT90S/LS2323 and AT90S/LS2323 and AT90S/LS2343. 8 bits are used to address the 128 bytes of SRAM in locations $60 - $DF.

Bit	7	6	5	4	3	2	1	0	
$3D ($5D)	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SPL
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt Stacks are located. This Stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer is decremented by one when data is pushed onto the Stack with the PUSH instruction, and it is decremented by two when data is pushed onto the Stack with subroutine CALL and interrupt. The Stack Pointer is incremented by one when data is popped from the Stack with the POP instruction, and it is incremented by two when data is popped from the Stack with return from subroutine RET or return from interrupt RETI.

Reset and Interrupt Handling

The AT90S/LS2323 and AT90S/LS2343 provides two interrupt sources. These interrupts and the separate reset vector, each have a separate program vector in the program memory space. Both interrupts are assigned individual enable bits which must be set (one) together with the I-bit in the status register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2 . The list also determines the priority levels of the interrupts. The lower the address the higher is the priority level. RESET has the highest priority, and next is INT0 - the External Interrupt Request 0, etc.

Table 2. Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	$000	RESET	Hardware Pin and Watchdog Reset
2	$001	INT0	External Interrupt Request 0
3	$002	TIMER0, OVF0	Timer/Counter0 Overflow

The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```
Address     Labels     Code             Comments
$000                   rjmp RESET       ; Reset Handler
$001                   rjmp EXT_INT0    ; IRQ0 Handler
$002                   rjmp TIM_OVF0    ; Timer0 Overflow Handler;
$003        MAIN:      <instr> xxx      ; Main program start
 …           …          …                …
```

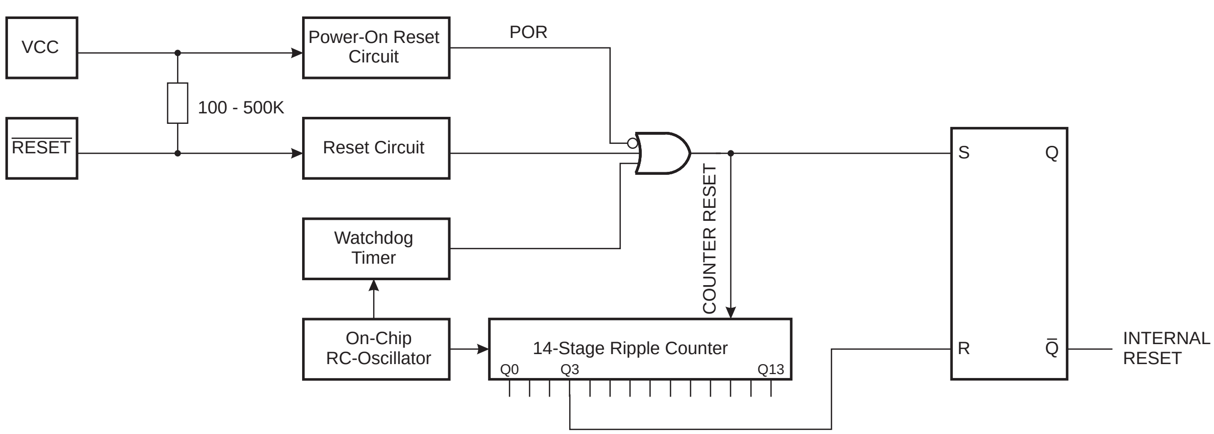
Reset Sources

The AT90S/LS2323 and AT90S/LS2343 provides three sources of reset:

- Power-On Reset. The MCU is reset when a supply voltage is applied to the VCC and GND pins.
- External Reset. The MCU is reset when a low level is present on the $\overline{\text{RESET}}$ pin for more than two XTAL cycles.
- Watchdog Reset. The MCU is reset when the Watchdog timer period expires and the Watchdog is enabled.

During reset, all I/O registers are set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP - relative jump - instruction to the reset handling routine. If the program never enables an interrupt source, the interrupt vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 24 shows the reset logic. Table 3 defines the timing and electrical parameters of the reset circuitry.

Figure 24. Reset Logic



The AT90S/LS2323 has a programmable startup time. A fuse bit - FSTRT - in the Flash memory selects the shortest startup time when programmed (‘0’). The AT90S/LS2323 is shipped with this bit unprogrammed.

The AT90S/LS2343 has a fixed startup time.

Table 3. Reset Characteristics (V_{CC} = 5.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}	Power-On Reset Threshold Voltage	1.1	1.3	1.5	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V
t_{TOUT}	Reset delay time-out period AT90S/LS2323 FSTRT programmed	1.0	1.1	1.2	ms
t_{TOUT}	Reset delay time-out period AT90S/LS2323 FSTRT unprogrammed	11	16	21	ms
t_{TOUT}	Reset Delay Time-Out Period AT90S/LS2343	11	16	21	µs

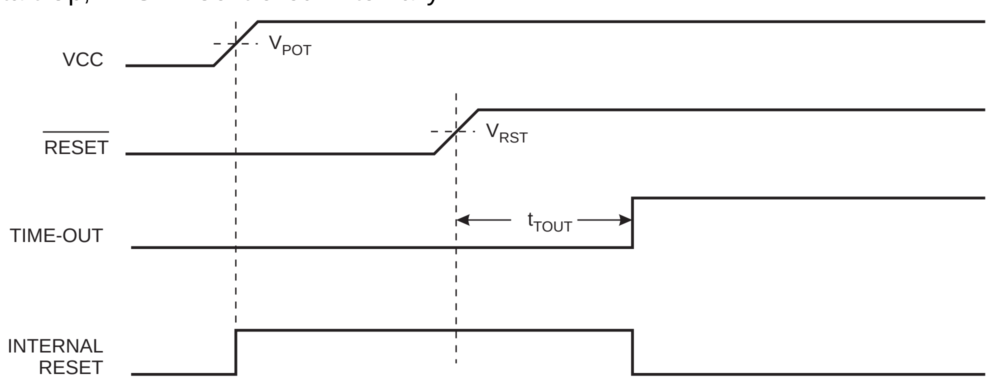
Table 4. Reset Characteristics (V_{CC} = 3.0V)

Symbol	Parameter	Min	Typ	Max	Units
V_{POT}	Power-On Reset Threshold Voltage	1.1	1.3	1.5	V
V_{RST}	$\overline{\text{RESET}}$ Pin Threshold Voltage		0.6 V_{CC}		V
t_{TOUT}	Reset delay time-out period AT90S/LS2323 FSTRT programmed	2.0	2.2	2.4	ms
t_{TOUT}	Reset delay time-out period AT90S/LS2323 FSTRT unprogrammed	22	32	42	ms
t_{TOUT}	Reset Delay Time-Out Period AT90S/LS2343	22	32	42	µs

Power-On Reset

The AT90S/LS2323 and AT90S/LS2343 is designed for use in systems where it can operate from the internal RC oscillator or in applications where a clock signal is provided by an external clock source. After V_{CC} has reached V_{POT}, the device will start after the time t_{TOUT}. If the clock signal is provided by an external clock source, the clock must not be applied until V_{CC} has reached the minimum voltage defined for the applied frequency.

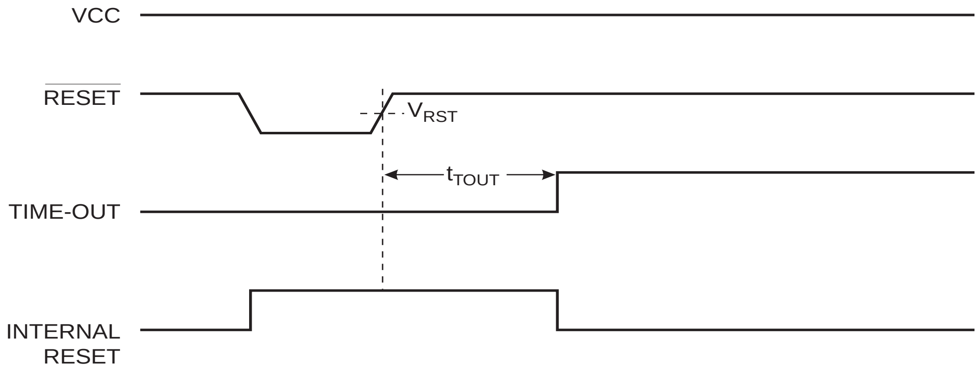
Figure 25. MCU Start-Up, $\overline{\text{RESET}}$ Controlled Externally



External Reset

An external reset is generated by a low level on the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin must be held low for at least two CPU-CLOCK clock cycles. When the applied signal reaches the Reset Threshold Voltage - V_{RST} on its positive edge, the delay timer starts the MCU after the Time-out period t_{TOUT} has expired.

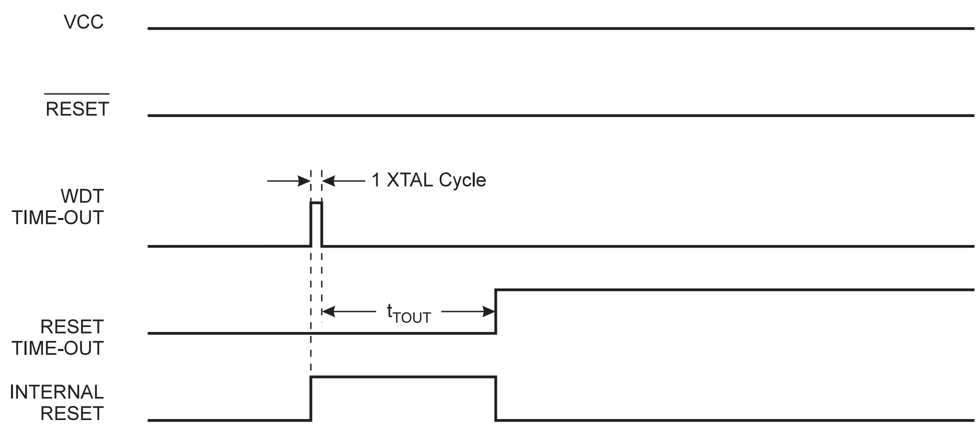
Figure 26. External Reset During Operation



Watchdog Reset

When the Watchdog times out, it will generate a short reset pulse of 1 XTAL cycle duration. On the falling edge of this pulse, the delay timer starts counting the Time-out period t_{TOUT}. Refer to page 21 for details on operation of the Watchdog.

Figure 27. Watchdog Reset During Operation



The MCU Status Register - MCUSR

The MCU Status Register provides information on which reset source caused a MCU reset:

Bit	7	6	5	4	3	2	1	0	
$34 ($54)	-	-	-	-	-	-	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R	R	R	R/W	R/W	
Initial value	0	0	0	0	0	0	See bit description		

- **Bit 7..2 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read as zero.

- **Bit 1 - EXTRF: External Reset Flag**

After a power-on reset, this bit is undefined (X). It will be set by an external reset. A watchdog reset will leave this bit unchanged.

- **Bit 0 - PORF: Power On Reset Flag**

This bit is set by a power-on reset. A watchdog reset or an external reset will leave this bit unchanged.

To summarize, the following table shows the value of these two bits after the three modes of reset.

Table 5. PORF and EXTRF Values after Reset

Reset Source	PORF	EXTRF
Power-On Reset	1	undefined
External Reset	unchanged	1
Watchdog Reset	unchanged	unchanged

To make use of these bits to identify a reset condition, the user software should clear both the PORF and EXTRF bits as early as possible in the program. Checking the PORF and EXTRF values is done before the bits are cleared. If the bit is cleared before an external or watchdog reset occurs, the source of reset can be found by using the following truth table:

Table 6. Reset Source Identification

PORF	EXTRF	Reset Source
0	0	Watchdog Reset
0	1	External Reset
1	0	Power-On Reset
1	1	Power-On Reset

Interrupt Handling

The AT90S/LS2323 and AT90S/LS2343 has two 8-bit Interrupt Mask control registers; GIMSK - General Interrupt Mask register and TIMSK - Timer/Counter Interrupt Mask register.

When an interrupt occurs, the Global Interrupt Enable I-bit is cleared (zero) and all interrupts are disabled. The user software can set (one) the I-bit to enable interrupts. The I-bit is set (one) when a Return from Interrupt instruction - RETI - is executed.

When the Program Counter is vectored to the actual interrupt vector in order to execute the interrupt handling routine, hardware clears the corresponding flag that generated the interrupt. Some of the interrupt flags can also be cleared by writing a logic one to the flag bit position(s) to be cleared.

The General Interrupt Mask Register - GIMSK

Bit	7	6	5	4	3	2	1	0	
$3B ($5B)	-	INT0	-	-	-	-	-	-	GIMSK
Read/Write	R	R/W	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - Res: Reserved Bit**

This bit is a reserved bit in the AT90S/LS2323 and AT90S/LS2343 and always reads as zero.

- **Bit 6 - INT0: External Interrupt Request 0 Enable**

When the INT0 bit is set (one) and the I-bit in the Status Register (SREG) is set (one), the external pin interrupt is activated. The Interrupt Sense Control0 bits 1/0 (ISC01 and ISC00) in the MCU general Control Register (MCUCR) defines whether the external interrupt is activated on rising or falling edge of the INT0 pin or level sensed. Activity on the pin will cause an interrupt request even if INT0 is configured as an output. The corresponding interrupt of External Interrupt Request 0 is executed from program memory address $001. See also “External Interrupts.”

- **Bits 5..0 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read as zero.

The General Interrupt Flag Register - GIFR

Bit	7	6	5	4	3	2	1	0	
$3A ($5A)	-	INTF0	-	-	-	-	-	-	GIFR
Read/Write	R	R/W	R	R	R	R	R	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - Res: Reserved Bit**

This bit is a reserved bit in the AT90S/LS2323 and AT90S/LS2343 and always reads as zero.

- **Bit 6 - INTF0: External Interrupt Flag0**

When an event on the INT0 pin triggers an interrupt request, INTF0 becomes set (one). If the I-bit in SREG and the INT0 bit in GIMSK are set (one), the MCU will jump to the interrupt vector at address $001. The flag is cleared when the interrupt routine is executed. Alternatively, the flag can be cleared by writing a logical one to it.

- **Bits 5..0 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read as zero.

The Timer/Counter Interrupt Mask Register - TIMSK

Bit	7	6	5	4	3	2	1	0	
$39 ($59)	-	-	-	-	-	-	TOIE0	-	TIMSK
Read/Write	R	R	R	R	R	R	R/W	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7..2 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read zero.

- **Bit 1 - TOIE0: Timer/Counter0 Overflow Interrupt Enable**

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt (at vector $002) is executed if an overflow in Timer/Counter0 occurs. The Overflow Flag (Timer0) is set (one) in the Timer/Counter Interrupt Flag Register - TIFR.

- **Bit 0 - Res: Reserved Bit**

This bit is a reserved bit in the AT90S/LS2323 and AT90S/LS2343 and always reads as zero.

The Timer/Counter Interrupt FLAG Register - TIFR

Bit	7	6	5	4	3	2	1	0	
$38 ($58)	-	-	-	-	-	-	TOV0	-	TIFR
Read/Write	R	R	R	R	R	R	R/W	R	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7..2 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read zero.

- **Bit 1 - TOV0: Timer/Counter0 Overflow Flag**

The bit TOV0 is set (one) when an overflow occurs in Timer/Counter0. TOV0 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV0 is cleared by writing a logical one to the flag. When the SREG I-bit, and TOIE0 (Timer/Counter0 Overflow Interrupt Enable), and TOV0 are set (one), the Timer/Counter0 Overflow interrupt is executed.

- **Bit 0 - Res: Reserved Bit**

This bit is a reserved bit in the AT90S/LS2323 and AT90S/LS2343 and always reads zero.

External Interrupt

The external interrupt is triggered by the INT0 pin. Observe that, if enabled, the interrupt will trigger even if the INT0 pin is configured as an output. This feature provides a way of generating a software interrupt. The external interrupt can be triggered by a falling or rising edge or a low level. This is set up as indicated in the specification for the MCU Control Register - MCUCR. When the external interrupt is enabled and is configured as level triggered, the interrupt will trigger as long as the pin is held low.

The external interrupt is set up as described in the specification for the MCU Control Register - MCUCR.

Interrupt Response Time

The interrupt execution response for all the enabled *AVR* interrupts is 4 clock cycles minimum. 4 clock cycles after the interrupt flag has been set, the program vector address for the actual interrupt handling routine is executed. During this 4 clock cycle period, the Program Counter (2 bytes) is pushed onto the Stack, and the Stack Pointer is decremented by 2. The vector is a relative jump to the interrupt routine, and this jump takes 2 clock cycles. If an interrupt occurs during execution of a multi-cycle instruction, this instruction is completed before the interrupt is served.

A return from an interrupt handling routine (same as for a subroutine call routine) takes 4 clock cycles. During these 4 clock cycles, the Program Counter (2 bytes) is popped back from the Stack, and the Stack Pointer is incremented by 2. When the *AVR* exits from an interrupt, it will always return to the main program and execute one more instruction before any pending interrupt is served.

Note that the Status Register - SREG - is not handled by the *AVR* hardware, neither for interrupts nor for subroutines. For the routines requiring a storage of the SREG, this must be performed by user software.

The MCU Control Register - MCUCR

The MCU Control Register contains control bits for general MCU functions.

Bit	7	6	5	4	3	2	1	0	
$35 ($55)	-	-	SE	SM	-	-	ISC01	ISC00	MCUCR
Read/Write	R	R	R/W	R/W	R	R	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

• **Bits 7, 6 - Res: Reserved Bits**
These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and always read as zero.

• **Bit 5 - SE: Sleep Enable**
The SE bit must be set (one) to make the MCU enter the sleep mode when the SLEEP instruction is executed. To avoid the MCU entering the sleep mode unless it is the programmers purpose, it is recommended to set the Sleep Enable SE bit just before the execution of the SLEEP instruction.

• **Bit 4 - SM: Sleep Mode**
This bit selects between the two available sleep modes. When SM is cleared (zero), Idle Mode is selected as Sleep Mode. When SM is set (one), Power Down mode is selected as sleep mode. For details, refer to the section “Sleep Modes” on page 19.

• **Bits 3, 2 - Res: Reserved Bits**
These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343, and always read as zero.

• **Bits 1, 0 - ISC01, ISC00: Interrupt Sense Control 0 Bit 1 and Bit 0**
The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask is set. The level and edges on the external INT0 pin that activate the interrupt are defined in the following table:

Table 7. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Note: When changing the ISC10/ISC00 bits, INT0 must be disabled by clearing its Interrupt Enable bit in the GIMSK Register. Otherwise an interrupt can occur when the bits are changed.

Sleep Modes

To enter the sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU awakes, executes the interrupt routine, and resumes execution from the instruction following SLEEP. The contents of the register file, SRAM and I/O memory are unaltered. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset vector.

Idle Mode

When the SM bit is cleared (zero), the SLEEP instruction forces the MCU into the Idle Mode stopping the CPU but allowing Timer/Counters, Watchdog and the interrupt system to continue operating. This enables the MCU to wake up from external triggered interrupts as well as internal ones like Timer Overflow interrupt and watchdog reset.

Power Down Mode

When the SM bit is set (one), the SLEEP instruction forces the MCU into the Power Down Mode. In this mode, the entire device is stopped. The user can select whether the watchdog shall be enabled during power-down mode. If the watchdog is enabled, it will wake up (and reset) the MCU when the Watchdog Time-out period expires. If the watchdog is disabled, only an external reset or an external level triggered interrupt can wake up the MCU. Note that when a level triggered interrupt is used for wake-up from power down, the low level must be held for a time longer than the reset delay time-out period t_{TOUT}. Otherwise, the device will not wake up.

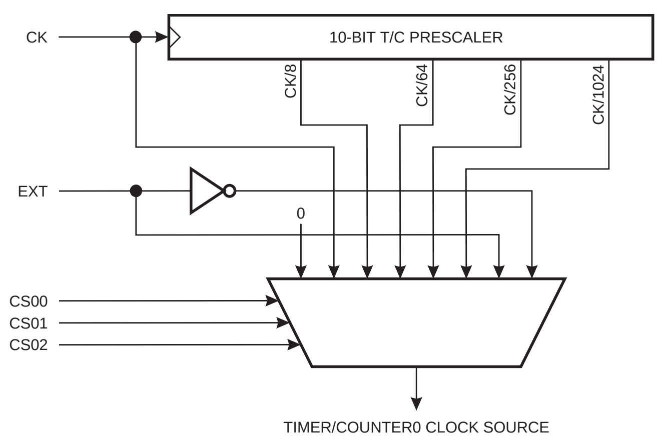
Timer/Counter

The AT90S/LS2323 and AT90S/LS2343 provides one general purpose 8- bit Timer/Counter - Timer/Counter0. The Timer/Counter has prescaling selection from the 10-bit prescaling timer. The Timer/Counter can either be used as a timer with an internal clock timebase or as a counter with an external pin connection that triggers the counting.

The Timer/Counter Prescaler

Figure 28 shows the Timer/Counter prescaler.

Figure 28. Timer/Counter0 Prescaler



The four different prescaled selections are: CK/8, CK/64, CK/256 and CK/1024 where CK is the oscillator clock. CK, external source and stop, can also be selected as clock sources.

The 8-Bit Timer/Counter0

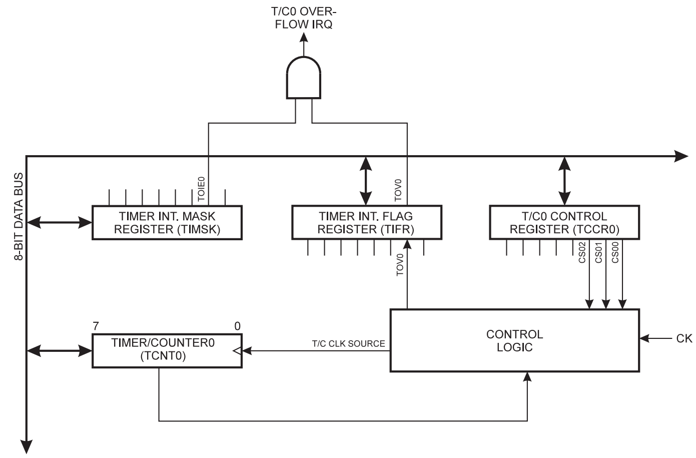
Figure 29 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK, or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter0 Control Register - TCCR0. The overflow status flag is found in the Timer/Counter Interrupt Flag Register - TIFR. Control signals are found in the Timer/Counter0 Control Register - TCCR0. The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register - TIMSK.

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To ensure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high resolution and a high accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

Figure 29. Timer/Counter 0 Block Diagram



The Timer/Counter0 Control Register - TCCR0

Bit	7	6	5	4	3	2	1	0	
$33 ($53)	-	-	-	-	-	CS02	CS01	CS00	TCCR0
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7..3 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343, and always read zero.

- **Bits 2,1,0 - CS02, CS01, CS00: Clock Select0, Bit 2,1 and 0**

The Clock Select0 bits 2,1 and 0 define the prescaling source of Timer0.

Table 8. Clock 0 Prescale Select

CS02	CS01	CS00	Description
0	0	0	Stop, the Timer/Counter0 is stopped.
0	0	1	CK
0	1	0	CK / 8
0	1	1	CK / 64
1	0	0	CK / 256
1	0	1	CK / 1024
1	1	0	External Pin T0, falling edge
1	1	1	External Pin T0, rising edge

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used, the corresponding setup must be performed in the actual data direction control register (cleared to zero gives an input pin).

The Timer Counter 0 - TCNT0

Bit	7	6	5	4	3	2	1	0	
$32 ($52)	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

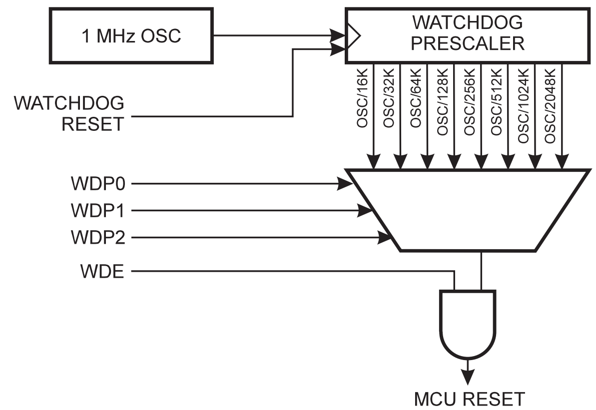
The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the timer clock cycle following the write operation.

The Watchdog Timer

The Watchdog Timer is clocked from a separate on-chip oscillator which runs at 1MHz. This is the typical value at V_{CC} = 5V. See characterization data for typical values at other V_{CC} levels. By controlling the Watchdog Timer prescaler, the Watchdog reset interval can be adjusted from 16K to 2,048K cycles (nominally 16 - 2048 ms). The WDR - Watchdog Reset - instruction resets the Watchdog Timer. Eight different clock cycle periods can be selected to determine the reset period. If the reset period expires without another Watchdog reset, the AT90S/LS2323 and AT90S/LS2343 resets and executes from the reset vector. For timing details on the Watchdog reset, refer to page 16.

To prevent unintentional disabling of the watchdog, a special turn-off sequence must be followed when the watchdog is disabled. Refer to the description of the Watchdog Timer Control Register for details.

Figure 30. Watchdog Timer



The Watchdog Timer Control Register - WDTCR

Bit	7	6	5	4	3	2	1	0	
$21 ($41)	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	WDTCR
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bits 7..5 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and will always read as zero.

- **Bit 4 - WDTOE: Watch Dog Turn-Off Enable**

This bit must be set (one) when the WDE bit is cleared. Otherwise, the watchdog will not be disabled. Once set, hardware will clear this bit to zero after four clock cycles. Refer to the description of the WDE bit for a watchdog disable procedure.

- **Bit 3 - WDE: Watch Dog Enable**

When the WDE is set (one) the Watchdog Timer is enabled, and if the WDE is cleared (zero) the Watchdog Timer function is disabled. WDE can only be cleared if the WDTOE bit is set(one). To disable an enabled watchdog timer, the following procedure must be followed:

1. In the same operation, write a logical one to WDTOE and WDE. A logical one must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logical 0 to WDE. This disables the watchdog.

- **Bits 2..0 - WDP2, WDP1, WDP0: Watchdog Timer Prescaler 1 and 0**

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding time-out periods are shown in Table 9 .

Table 9. Watch Dog Timer Prescale Select

WDP2	WDP1	WDP0	Time-out Period
0	0	0	16K cycles
0	0	1	32K cycles
0	1	0	64K cycles
0	1	1	128K cycles
1	0	0	256K cycles
1	0	1	512K cycles
1	1	0	1,024K cycles
1	1	1	2,048K cycles

EEPROM Read/Write Access

The EEPROM access registers are accessible in the I/O space.

The write access time is in the range of 2.5 - 4ms, depending on the V_{CC} voltages. A self-timing function, however, lets the user software detect when the next byte can be written.

In order to prevent unintentional EEPROM writes, a specific write procedure must be followed. Refer to the description of the EEPROM Control Register for details on this.

When the EEPROM is read or written, the CPU is halted for two clock cycles before the next instruction is executed.

The EEPROM Address Register - EEAR

Bit	7	6	5	4	3	2	1	0	
$1E ($3E)	-	EEAR6	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	EEAR
Read/Write	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7 - Res: Reserved Bit**

This bit is a reserved bit in the AT90S/LS2323 and AT90S/LS2343 and will always read as zero.

- **Bit 6..0 - EEAR6..0: EEPROM Address**

The EEPROM Address Register - EEAR6..0 - specifies the EEPROM address in the 128 bytes EEPROM space. The EEPROM data bytes are addressed linearly between 0 and 127.

The EEPROM Data Register - EEDR

Bit	7	6	5	4	3	2	1	0	
$1D ($3D)	MSB							LSB	EEDR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7..0 - EEDR7..0: EEPROM Data**

For the EEPROM write operation, the EEDR register contains the data to be written to the EEPROM in the address given by the EEAR register. For the EEPROM read operation, the EEDR contains the data read out from the EEPROM at the address given by EEAR.

The EEPROM Control Register - EECR

Bit	7	6	5	4	3	2	1	0	
$1C ($3C)	-	-	-	-	-	EEMWE	EEWE	EERE	EECR
Read/Write	R	R	R	R	R	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

- **Bit 7..3 - Res: Reserved Bits**

These bits are reserved bits in the AT90S/LS2323 and AT90S/LS2343 and will always read as zero.

- **Bit 2 - EEMWE: EEPROM Master Write Enable**

The EEMWE bit determines whether setting EEWE to one causes the EEPROM to be written. When EEMWE is set(one) setting EEWE will write data to the EEPROM at the selected address. If EEMWE is zero, setting EEWE will have no effect. When EEMWE has been set (one) by software, hardware clears the bit to zero after four clock cycles. See the description of the EEWE bit for a EEPROM write procedure.

- **Bit 1 - EEWE: EEPROM Write Enable**

The EEPROM Write Enable Signal EEWE is the write strobe to the EEPROM. When address and data are correctly set up, the EEWE bit must be set to write the value into the EEPROM. The EEMWE bit must be set when the logical one is written to EEWE, otherwise no EEPROM write takes place. The following procedure should be followed when writing the EEPROM (the order of steps 2 and 3 is unessential):

1. Wait until EEWE becomes zero
2. Write new EEPROM address to EEAR (optional)
3. Write new EEPROM data to EEDR (optional)
4. Write a logical one to the EEMWE bit in EECR
5. Within four clock cycles after setting EEMWE, write a logical one to EEWE

When the write access time (typically 2.5 ms at V_{CC} = 5V or 4 ms at V_{CC} = 2.7V) has elapsed, the EEWE bit is cleared (zero) by hardware. The user software can poll this bit and wait for a zero before writing the next byte. When EEWE has been set, the CPU is halted for two cycles before the next instruction is executed.

- **Bit 0 - EERE: EEPROM Read Enable**

The EEPROM Read Enable Signal EERE is the read strobe to the EEPROM. When the correct address is set up in the EEAR register, the EERE bit must be set. When the EERE bit is cleared (zero) by hardware, requested data is found in the EEDR register. The EEPROM read access takes one instruction and there is no need to poll the EERE bit. When EERE has been set, the CPU is halted for two cycles before the next instruction is executed.

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress when new data or address is written to the EEPROM I/O registers, the write operation will be interrupted, and the result is undefined.

I/O Port B

For the AT90S/LS2323, port B is an 3-bit bi-directional I/O port. For the AT90S/LS2343, port B is a 5-bit bi-directional I/O port.

Please note: bits 3 and 4 in the description of PORTB, DDRB, and PINB do not apply to the AT90S/LS2323. They are read only with a value of 0.

Three data memory address locations are allocated for Port B, one each for the Data Register - PORTB, $18 ($38), Data Direction Register - DDRB, $17($37) and the Port B Input Pins - PINB, $16($36). The Port B Input Pins address is read only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20mA and thus drive LED displays directly. When pins PB0 to PB4 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in the following table:

Table 10. Port B Pins Alternate Functions

Port Pin	Alternate Functions
PB0	MOSI (Data input line for memory downloading)
PB1	MISO (Data output line for memory uploading) INT0 (External Interrupt0 Input)
PB2	SCK (Serial clock input for serial programming) TO (Timer/Counter0 counter clock input)
PB3	CLOCK (Clock input, AT90S/LS2343 only)

When the pins are used for the alternate function the DDRB and PORTB register has to be set according to the alternate function description.

The Port B Data Register - PORTB

Bit	7	6	5	4	3	2	1	0	
$18 ($38)	-	-	-	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Port B Data Direction Register - DDRB

Bit	7	6	5	4	3	2	1	0	
$17 ($37)	-	-	-	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R	R	R	R/W	R/W	R/W	R/W	R/W	
Initial value	0	0	0	0	0	0	0	0	

The Port B Input Pins Address - PINB

Bit	7	6	5	4	3	2	1	0	
$16 ($36)	-	-	-	PINB4	PINB3	PINB2	PINB1	PINB0	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial value	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	

The Port B Input Pins address - PINB - is not a register, and this address enables access to the physical value on each Port B pin. When reading PORTB, the PORTB Data Latch is read, and when reading PINB, the logical values present on the pins are read.

PORTB as General Digital I/O

All bits in port B are equal when used as digital I/O pins.

PBn, General I/O pin: The DDBn bit in the DDRB register selects the direction of this pin, if DDBn is set (one), PBn is configured as an output pin. If DDBn is cleared (zero), PBn is configured as an input pin. If PORTBn is set (one) when the pin configured as an input pin, the MOS pull up resistor is activated. To switch the pull up resistor off, the PORTBn has to be cleared (zero) or the pin has to be configured as an output pin.

Table 11. DDBn Effects on Port B Pins

DDBn	PORTBn	I/O	Pull up	Comment
0	0	Input	No	Tri-state (Hi-Z)
0	1	Input	Yes	PBn will source current if ext. pulled low.
1	0	Output	No	Push-Pull Zero Output
1	1	Output	No	Push-Pull One Output

Alternate Functions of PORTB

The alternate pin functions of Port B are:

CLOCK - PORTB, Bit 3

Clock input: AT90S/LS2343 only. When the RCEN fuse is programmed and the device runs from the internal RC oscillator, this pin is a general I/O pin. When the RCEN Fuse is unprogrammed, an external clock source must be connected to CLOCK.

SCK/T0 - PORTB, Bit 2

In serial programming mode, this bit serves as the serial clock input, SCK.

During normal operation, this pin can serve as the external counter clock input. See the timer/counter description for further details. If external timer/counter clocking is selected, activity on this pin will clock the counter even if it is configured as an output.

MISO - PORTB, Bit 1

In serial programming mode, this bit serves as the serial data output, MISO.

During normal operation, this pin can serve as the external interrupt0 input. See the interrupt description for details on how to enable this interrupt. Note that activity on this pin will trigger the interrupt even if the pin is configured as an output.

MOSI - PORTB, Bit 0

In serial programming mode, this pin serves as the serial data input, MOSI.

Memory Programming

Program Memory Lock Bits

The AT90S/LS2323 and AT90S/LS2343 MCU provides two lock bits which can be left unprogrammed ('1') or can be programmed ('0') to obtain the additional features listed in Table 12 .

Table 12. Lock Bit Protection Modes

Program Lock Bits			
Mode	**LB1**	**LB2**	**Protection Type**
1	1	1	No program lock features
2	0	1	Further programming of the Flash and EEPROM is disabled
3	0	0	Same as mode 2, but verify is also disabled.

Note: The Lock Bits can only be erased with the Chip Erase operation.

Fuse Bits

The AT90S/LS2323 has two fuse bits, SPIEN and RCEN. The AT90A/LS2343 has the SPIEN fuse only.

- When SPIEN is programmed ('0'), Serial Program Downloading is enabled. Default value is programmed ('0'). This bit is not accessible in the serial programming mode.
- When RCEN is programmed ('0'), the internal RC oscillator is selected as the MCU clock source. Default value is programmed ('0'). When the status of this bit is changed in serial mode, the change occurs on the next power-on reset.

Neither of these bits are affected by a chip erase.

Signature Bytes

All Atmel microcontrollers have a three-byte signature code which identifies the device. The three bytes reside in a separate address space, and for the AT90S/LS2323 and AT90S/LS2343 they are:

1. \$00: \$1E (indicates manufactured by Atmel)
2. \$01: \$91 (indicates 2K bytes Flash memory)
3. \$02: \$03 or \$04 (Indicates 90S/LS2343 when \$01 is \$97 and \$02 is \$03. Indicates 90S/LS2323 when \$01 is \$97 and \$02 is \$04.)

In serial mode, the signature bytes can not be read if lock mode 3 is enabled, i.e. both lock bits are programmed. In this case, the +12V Special Programming mode must be used.

Programming the Flash and EEPROM

Atmel's AT90S/LS2323 and AT90S/LS2343 offers 2K bytes of in-system programmable Flash Program memory and 128 bytes of EEPROM Data memory.

The AT90S/LS2323 and AT90S/LS2343 is normally shipped with the on-chip Flash Program and EEPROM Data memory arrays in the erased state (i.e., contents = \$FF) and ready to be programmed. The device supports a Low-Voltage Serial programming mode. This mode provides a convenient way to download the Program and Data into the AT90S/LS2323 and AT90S/LS2343 inside the user's system.

The Program and EEPROM memory arrays in the AT90S/LS2323 and AT90S/LS2343 are programmed byte-by-byte in either programming modes. For the EEPROM, an auto-erase cycle is provided with the self-timed programming operation in the serial programming mode.

Some functions that are not accessible in serial programming mode, have to be performed in a +12V Special Programming mode. The +12V is used for programming enable only, and no current of significance is drawn by this pin.

+12V Special Programming Mode

This mode is used to perform functions that are not available in serial programming mode. These are:

- Read Signature bytes in lock mode 3

- Program/Unprogram the SPIEN fuse.

All shift operations described are MSB first and use the CLOCK/XTAL1 pin as the clock.

Enter Special Programming Mode

1. Apply 4.5 - 5.5V between VCC and GND
2. Set $\overline{\text{RESET}}$ and PB0 to '0'
3. Toggle CLOCK/XTAL1 at least 8 times and leave it low('0')
4. Wait at least 100 ns.
5. Apply 12V to $\overline{\text{RESET}}$ and wait at least 100 ns.

Reading the Signature Bytes

1. Give CLOCK a positive pulse
2. Shift simultaneously the following values into PB0 and PB1: (Send MSB first, use CLOCK/XTAL1 as the shift clock)
   PB0:'0000 1000'
   PB1:'0100 1100'
3. Apply 3 positive pulses to CLOCK/XTAL1
4. Shift in simultaneously:
   PB0:'0000 0000' This is the address of signature byte #0
   PB1:'0000 1100'
5. Apply 3 positive pulses to CLOCK/XTAL1
6. Shift '0110 1000' into PB1
7. Apply 2 positive pulses to CLOCK/XTAL1
8. Shift signature byte 0 out from PB2
9. Apply 4 positive pulses to CLOCK/XTAL1
10. Shift '0110 1100' into PB1
11. Repeat Steps 3 - 10 using addresses '0000 0001' and '0000 0010' for the following two signature bytes in Step 8
12. Apply 2 positive pulses to CLOCK/XTAL1

Programming the Fuse Bits

1. Give CLOCK/XTAL1 a positive pulse
2. Shift in simultaneously:
   PB0:'0100 0000'
   PB1:'0100 1100'
3. Apply 3 positive pulses to CLOCK/XTAL1
4. Shift in simultaneously:
   PB0:'00S0 000R'. S/R='1': SPIEN/RCEN unprogrammed, S/R='0' SPIEN/RCEN programmed
   PB1:'0010 1100'
5. Apply 3 positive pulses to CLOCK/XTAL1
6. Shift '0110 0100' into PB1
7. Apply 2 positive pulses to CLOCK/XTAL1
8. Wait 1 ms
9. Give CLOCK/XTAL1 a positive pulse
10. Shift '0110 1100' into PB1
11. Apply 2 positive pulses to CLOCK/XTAL1

Reading the Fuse and Lock Bits

1. Give CLOCK/XTAL1 a positive pulse
2. Shift in simultaneously:
   PB0:'0000 0100'
   PB1:'0100 1100'
3. Apply 3 positive pulses to CLOCK/XTAL1
4. Shift '0111 1000' into PB1
5. Apply 2 positive pulses to CLOCK/XTAL1
6. Shift data out of PB2. The status of the fuse and lock bits is found in the following bits:
   Bit 7: Lock Bit1 ('0' means programmed)
   Bit 6: Lock Bit2 ('0' means programmed)
   Bit 5: SPIEN Fuse ('0' means programmed, '1' means unprogrammed)
   Bit 0: RCEN Fuse ('0' means programmed, '1' means unprogrammed)
7. Apply 4 positive pulses to CLOCK/XTAL1
8. Shift '0111 1100' into PB1
9. Apply 2 positive pulses to CLOCK/XTAL1

Low Voltage Serial Programming

Both the Program and Data memory arrays can be programmed using the serial SPI bus while $\overline{\text{RESET}}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After $\overline{\text{RESET}}$ is set low, the Programming Enable instruction needs to be executed first before program/erase operations can be executed.

When programming the EEPROM, an auto-erase cycle is built into the self-timed programming operation (in the serial mode ONLY) and there is no need to first execute the Chip Erase instruction. The Chip Erase operation turns the content of every memory location in both the Program and EEPROM arrays into $FF.

The Program and EEPROM memory arrays have separate address spaces, $000 to $3FF for Program Flash memory and $000 to $07F for EEPROM Data memory.

Either an external system clock is applied to the CLOCK/XTAL1 pin or the device must be clocked from the internal RC-oscillator. The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 MCU clock cycles

High: > 2 MCU clock cycles

Serial Programming Algorithm

To program and verify the AT90S/LS2323 and AT90S/LS2343 in the serial programming mode, the following sequence is recommended (See four byte instruction formats in Table 13):

1. Power-up sequence:

   Apply power between VCC and GND while RESET and SCK are set to ‘0’. (If the programmer can not guarantee that SCK is held low during power-up, RESET must be given a positive pulse after SCK has been set to ‘0’.) If the device is programmed for external clocking, apply a 0 to 8 MHz clock to the CLOCK/XTAL1 pin. If the internal RC oscillator is selected as the clock source, no external clock source needs to be applied.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to pin MOSI/PB0. Refer to the above section for minimum low and high periods for the serial clock input, SCK.
3. If a chip erase is performed (must be done to erase the Flash), wait 10 ms, give $\overline{\text{RESET}}$ a positive pulse and start over again from Step 2.
4. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate Write instruction. An EEPROM memory location is first automatically erased before new data is written. The next byte can be written after 4 ms.
5. Any memory location can be verified by using the Read instruction which returns the content at the selected address at serial output MISO/PB1.

At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.

6. Power-off sequence (if needed):

   Set CLOCK/XTAL1 to ‘0’.

   Set $\overline{\text{RESET}}$ to ‘1’.

   Turn V_{CC} power off.

Table 13. Serial Programming Instruction Set AT90S/LS2323 and AT90S/LS2343

Instruction	Instruction Format				Operation
	Byte 1	Byte 2	Byte 3	Byte 4	
Programming Enable	1010 1100	0101 0011	xxxx xxxx	xxxx xxxx	Enable Serial Programming after $\overline{\text{RESET}}$ goes low
Chip Erase	1010 1100	100x xxxx	xxxx xxxx	xxxx xxxx	Chip erase both 2K & 128 byte memory arrays
Read Program Memory	0010 **H**000	0000 00**aa**	**bbbb bbbb**	**oooo oooo**	Read H (high or low) data o from Program memory at word address a:b
Write Program Memory	0100 **H**000	0000 00**aa**	**bbbb bbbb**	**iiii iiii**	Write H (high or low) data **i** to Program memory at word address a:b
Read EEPROM Memory	1010 0000	0000 0000	x**bbb bbbb**	**oooo oooo**	Read data o from EEPROM memory at address b
Write EEPROM Memory	1100 0000	0000 0000	x**bbb bbbb**	**iiii iiii**	Write data i to EEPROM memory at address b
Read Lock and Fuse Bits	0101 1000	xxxx xxxx	xxxx xxxx	***12*****S**x xxx**R**	Read lock and fuse bits. ‘0’: Programmed, ‘1’: Unprogrammed
Write Lock Bits	1010 1100	111x x***21***x	xxxx xxxx	xxxx xxxx	Write lock bits. Set bits 1,2=‘0’ to program lock bits.
Write RCEN Bit	1010 1100	101x xxx**R**	xxxx xxxx	xxxx xxxx	Write RCEN fuse. Set bit R=‘0’ to program fuse, ‘1’ to unprogram(3)
Read Device Code	0011 0000	xxxx xxxx	xxxx xx**bb**	**oooo oooo**	Read Device Code o from address b(2)

Notes: 1. **a** = address high bits
b = address low bits
H = 0 - Low byte, 1- High byte
o = data out
i = data in
x = don’t care
1 = lock bit 1
2 = lock bit 2
R = RCEN Fuse
S = SPIEN Fuse

2. The device code is not readable in lock mode 3, i.e. both lock bits programmed

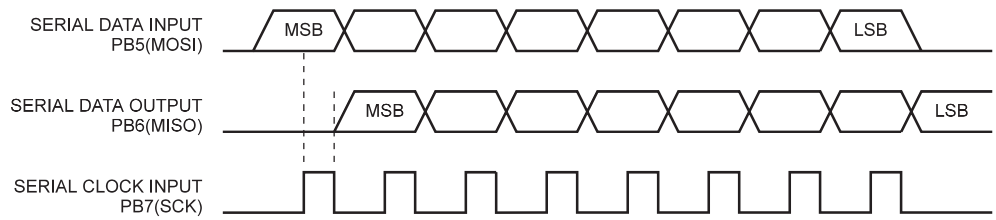
3. When the state of the RCEN bit is changed in serial programming mode, the device must be power cycled for the changes to have any effect

When writing serial data to the AT90S/LS2323 and AT90S/LS2343, data is clocked on the rising edge of CLK.

When reading data from the AT90S/LS2323 and AT90S/LS2343, data is clocked on the falling edge of CLK. See Figure 29 for an explanation.

Programming Characteristics

Figure 31. Serial Downloading Waveforms



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Current per I/O Pin	40.0 mA
DC Current VCC and GND Pins	140.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

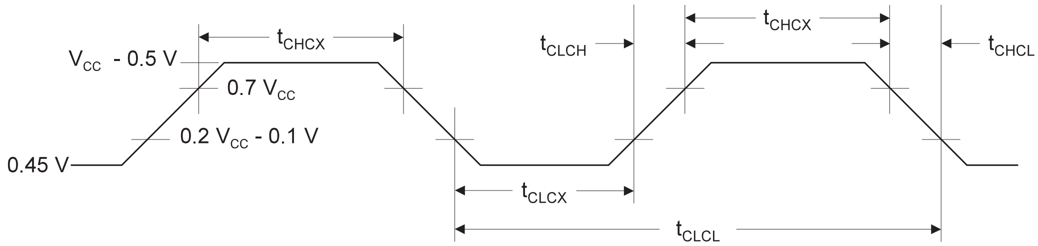
T_A = -40°C to 85°C, V_{CC} = 2.7V to 6.0V (unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IL}	Input Low Voltage		-0.5		0.3 V_{CC}	V
V_{IL1}	Input Low Voltage	XTAL	-0.5		0.1 V_{CC}	V
V_{IH}	Input High Voltage	(Except XTAL, RESET)	0.6 V_{CC}		V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	XTAL	0.7 V_{CC}		V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	RESET	0.85 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[1] Ports A, B, C, D	I_{OL} = 20 mA, V_{CC} = 5V I_{OL} = 10 mA, V_{CC} = 3V			0.6 0.5	V V
V_{OH}	Output High Voltage Ports A, B, C, D	I_{OH} = -3 mA, V_{CC} = 5V I_{OH} = -1.5 mA, V_{CC} = 3V	4.3 2.3			V V
I_{IL}	Input Leakage Current I/O Pin	V_{CC} = 6V, Pin Low	-8.0		8.0	µA
I_{IH}	Input Leakage Current I/O Pin	V_{CC} = 6V, Pin High	-8.0		8.0	µA
RRST	Reset Pullup		100		500	kΩ
$R_{I/O}$	I/O Pin Pullup		35		122	kΩ
I_{CC}	Power Supply Current	Active 4 MHz, 3 V_{CC}			3.0	mA
		Idle 4 MHz, 3 V_{CC}		1.0	1.2	mA
		Power Down 4 MHz[2], 3 V_{CC} WDT Enabled		9.0	15.0	µA
		Power Down 4 MHz[2], 3 V_{CC} WDT Disabled		<1	2.0	µA
V_{ACIO}	Analog Comp Input Offset V	V_{CC} = 5V			40	mV
I_{ACLK}	Analog Comp Input Leakage A	V_{CC} = 5V V_{IN} = V_{CC}/2	-50		50	nA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum total I_{OL} for all output pins: 80mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification.
Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

External Clock Drive Waveforms



External Clock Drive

T_A = -40°C to 85°C

Symbol	Parameter	AT90LS2323/43		AT90S2323/43		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency	0	4	0	10	MHz
t_{CLCL}	Clock Period	250		100		ns
t_{CHCX}	High Time	0		0		ns
t_{CLCX}	Low Time	0		0		ns
t_{CLCH}	Rise Time		1.6		0.5	µs
t_{CHCL}	Fall Time		1.6		0.5	µs

AT90S/LS2323 and AT90S/LS2343 Register Summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F ($5F)	SREG	I	T	H	S	V	N	Z	C	page 13
$3E ($5E)	Reserved									
$3D ($5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 13
$3C ($5C)	Reserved									
$3B ($5B)	GIMSK	-	INT0	-	-	-	-	-	-	page 17
$3A ($5A)	GIFR	-	INTF0							page 17
$39 ($59)	TIMSK	-	-	-	-	-	-	TOIE0	-	page 15
$38 ($58)	TIFR	-	-	-	-	-	-	TOV0	-	page 16
$37 ($57)	Reserved									
$36 ($56)	Reserved									
$35 ($55)	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00	page 16
$34 ($54)	MCUSR	-	-	-	-	-	-	EXTRF	PORF	page 14
$33 ($53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 20
$32 ($52)	TCNT0	Timer/Counter0 (8 Bit)								page 20
$31 ($51)	Reserved									
$30 ($50)	Reserved									
$2F ($4F)	Reserved									
$2E ($4E)	Reserved									
$2D ($4D)	Reserved									
$2C ($4C)	Reserved									
$2B ($4B)	Reserved									
$2A ($4A)	Reserved									
$29 ($49)	Reserved									
$28 ($48)	Reserved									
$27 ($47)	Reserved									
$26 ($46)	Reserved									
$25 ($45)	Reserved									
$24 ($44)	Reserved									
$23 ($43)	Reserved									
$22 ($42)	Reserved									
$21 ($41)	WDTCR	-	-	-	WDTO	WDE	WDP2	WDP1	WDP0	page 21
$20 ($40)	Reserved									
$1F ($3F)	Reserved									
$1E ($3E)	EEAR	-	EEPROM Address Register							page 22
$1D ($3D)	EEDR	EEPROM Data register								page 22
$1C ($3C)	EECR	-	-	-	-	-	EEMW	EEWE	EERE	page 22
$1B ($3B)	Reserved									
$1A ($3A)	Reserved									
$19 ($39)	Reserved									
$18 ($38)	PORTB	-	-	-	PORTB	PORTB	PORTB	PORTB	PORTB	page 23
$17 ($37)	DDRB	-	-	-	DDB4	DDB3	DDB2	DDB1	DDB0	page 23
$16 ($36)	PINB	-	-	-	PINB4	PINB3	PINB2	PINB1	PINB0	page 23
$15 ($35)	Reserved									
$14 ($34)	Reserved									
$13 ($33)	Reserved									
$12 ($32)	Reserved									
$11 ($31)	Reserved									
$10 ($30)	Reserved									
$0F ($2F)	Reserved									
$0E ($2E)	Reserved									
$0D ($2D)	Reserved									
$0C ($2C)	Reserved									
$0B ($2B)	Reserved									
$0A ($2A)	Reserved									
$09 ($29)	Reserved									
$08 ($28)	Reserved									
…	Reserved									
$00 ($20)	Reserved									

AT90S/LS2323 and AT90S/LS2343 Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clock
ARITHMETIC AND LOGIC INSTRUCTIONS					
ADD	Rd, Rr	Add two Registers	Rd ← Rd + Rr	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	Rd ← Rd + Rr + C	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	Rdh:Rdl ← Rdh:Rdl + K	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	Rd ← Rd − Rr	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	Rd ← Rd − K	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	Rdh:Rdl ← Rdh:Rdl − K	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry two Registers	Rd ← Rd − Rr − C	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	Rd ← Rd − K − C	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	Rd ← Rd • Rr	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	Rd ← Rd • K	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	Rd ← Rd v Rr	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	Rd ← Rd v K	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	Rd ← Rd ⊕ Rr	Z,N,V	1
COM	Rd	One's Complement	Rd ← $FF − Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← $00 − Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	Rd ← Rd v K	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	Rd ← Rd • ($FF − K)	Z,N,V	1
INC	Rd	Increment	Rd ← Rd + 1	Z,N,V	1
DEC	Rd	Decrement	Rd ← Rd − 1	Z,N,V	1
TST	Rd	Test for Zero or Minus	Rd ← Rd • Rd	Z,N,V	1
CLR	Rd	Clear Register	Rd ← Rd ⊕ Rd	Z,N,V	1
SER	Rd	Set Register	Rd ← $FF	None	1
BRANCH INSTRUCTIONS					
RJMP	k	Relative Jump	PC ← PC + k + 1	None	2
IJMP		Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	PC ← PC + k + 1	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK	I	4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC ← PC + 2 or 3	None	1 / 2
CP	Rd,Rr	Compare	Rd − Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd − Rr − C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd − K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC ← PC + 2 or 3	None	1 / 2
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b)=0) PC ← PC + 2 or 3	None	1 / 2
SBIS	P, b	Skip if Bit in I/O Register is Set	if (R(b)=1) PC ← PC + 2 or 3	None	1 / 2
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then PC←PC + k + 1	None	1 / 2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then PC←PC + k + 1	None	1 / 2
BREQ	k	Branch if Equal	if (Z = 1) then PC ← PC + k + 1	None	1 / 2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC ← PC + k + 1	None	1 / 2
BRCS	k	Branch if Carry Set	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRCC	k	Branch if Carry Cleared	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC ← PC + k + 1	None	1 / 2
BRLO	k	Branch if Lower	if (C = 1) then PC ← PC + k + 1	None	1 / 2
BRMI	k	Branch if Minus	if (N = 1) then PC ← PC + k + 1	None	1 / 2
BRPL	k	Branch if Plus	if (N = 0) then PC ← PC + k + 1	None	1 / 2
BRGE	k	Branch if Greater or Equal, Signed	if (N ⊕ V= 0) then PC ← PC + k + 1	None	1 / 2
BRLT	k	Branch if Less Than Zero, Signed	if (N ⊕ V= 1) then PC ← PC + k + 1	None	1 / 2
BRHS	k	Branch if Half Carry Flag Set	if (H = 1) then PC ← PC + k + 1	None	1 / 2
BRHC	k	Branch if Half Carry Flag Cleared	if (H = 0) then PC ← PC + k + 1	None	1 / 2
BRTS	k	Branch if T Flag Set	if (T = 1) then PC ← PC + k + 1	None	1 / 2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC ← PC + k + 1	None	1 / 2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC ← PC + k + 1	None	1 / 2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC ← PC + k + 1	None	1 / 2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC ← PC + k + 1	None	1 / 2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC ← PC + k + 1	None	1 / 2

(continued)

Mnemonics	Operands	Description	Operation	Flags	#Clocks
DATA TRANSFER INSTRUCTIONS					
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	Rd ← K	None	1
LD	Rd, X	Load Indirect	Rd ← (X)	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	Rd ← (X), X ← X + 1	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	X ← X - 1, Rd ← (X)	None	2
LD	Rd, Y	Load Indirect	Rd ← (Y)	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	Rd ← (Y), Y ← Y + 1	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	Y ← Y - 1, Rd ← (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	Rd ← (Y + q)	None	2
LD	Rd, Z	Load Indirect	Rd ← (Z)	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	Rd ← (Z), Z ← Z+1	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	Z ← Z - 1, Rd ← (Z)	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	Rd ← (Z + q)	None	2
LDS	Rd, k	Load Direct from SRAM	Rd ← (k)	None	2
ST	X, Rr	Store Indirect	(X) ← Rr	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	(X) ← Rr, X ← X + 1	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	X ← X - 1, (X) ← Rr	None	2
ST	Y, Rr	Store Indirect	(Y) ← Rr	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	(Y) ← Rr, Y ← Y + 1	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	Y ← Y - 1, (Y) ← Rr	None	2
STD	Y+q,Rr	Store Indirect with Displacement	(Y + q) ← Rr	None	2
ST	Z, Rr	Store Indirect	(Z) ← Rr	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	(Z) ← Rr, Z ← Z + 1	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	Z ← Z - 1, (Z) ← Rr	None	2
STD	Z+q,Rr	Store Indirect with Displacement	(Z + q) ← Rr	None	2
STS	k, Rr	Store Direct to SRAM	(k) ← Rr	None	2
LPM		Load Program Memory	R0 ← (Z)	None	3
IN	Rd, P	In Port	Rd ← P	None	1
OUT	P, Rr	Out Port	P ← Rr	None	1
PUSH	Rr	Push Register on Stack	STACK ← Rr	None	2
POP	Rd	Pop Register from Stack	Rd ← STACK	None	2
BIT AND BIT-TEST INSTRUCTIONS					
SBI	P,b	Set Bit in I/O Register	I/O(P,b) ← 1	None	2
CBI	P,b	Clear Bit in I/O Register	I/O(P,b) ← 0	None	2
LSL	Rd	Logical Shift Left	Rd(n+1) ← Rd(n), Rd(0) ← 0	Z,C,N,V	1
LSR	Rd	Logical Shift Right	Rd(n) ← Rd(n+1), Rd(7) ← 0	Z,C,N,V	1
ROL	Rd	Rotate Left Through Carry	Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7)	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0)	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	Rd(n) ← Rd(n+1), n=0..6	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0)	None	1
BSET	s	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	s	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)	T	1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	C	1
CLC		Clear Carry	C ← 0	C	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	Z ← 0	Z	1
SEI		Global Interrupt Enable	I ← 1	I	1
CLI		Global Interrupt Disable	I ← 0	I	1
SES		Set Signed Test Flag	S ← 1	S	1
CLS		Clear Signed Test Flag	S ← 0	S	1
SEV		Set Twos Complement Overflow	V ← 1	V	1
CLV		Clear Twos Complement Overflow	V ← 0	V	1
SET		Set T in SREG	T ← 1	T	1
CLT		Clear T in SREG	T ← 0	T	1
SEH		Set Half Carry Flag in SREG	H ← 1	H	1
CLH		Clear Half Carry Flag in SREG	H ← 0	H	1
NOP		No Operation		None	1
SLEEP		Sleep	(see specific descr. for Sleep	None	3
WDR		Watchdog Reset	(see specific descr. for WDR/timer)	None	1

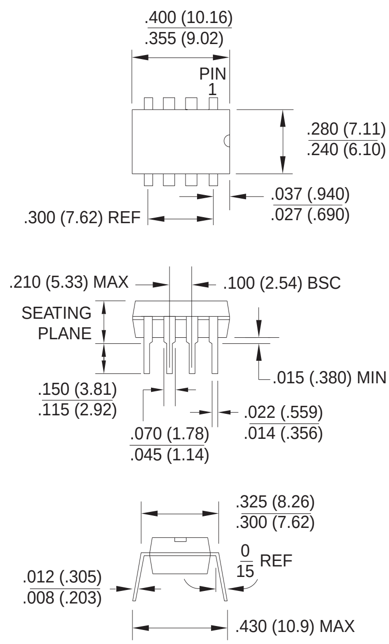
Ordering Information

Power Supply	Speed (MHz)	Ordering Code	Package	Operation Range
2.7 - 6.0V	4	AT90LS2343-4PC AT90LS2343-4SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90LS2343-4PI AT90LS2343-4SI	8P3 8S2	Industrial (-40°C to 85°C)
4.0 - 6.0V	10	AT90S2343-10PC AT90S2343-10SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90S2343-10PI AT90S2343-10SI	8P3 8S2	Industrial (-40°C to 85°C)
2.7 - 6.0V	4	AT90LS2323-4PC AT90LS2323-4SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90LS2323-4PI AT90LS2323-4SI	8P3 8S2	Industrial (-40°C to 85°C)
4.0 - 6.0V	10	AT90S2323-10PC AT90S2323-10SC	8P3 8S2	Commercial (0°C to 70°C)
		AT90S2323-10PI AT90S2323-10SI	8P3 8S2	Industrial (-40°C to 85°C)

Package Type	
8P3	8-Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
8S2	8-Lead, 0.200" Wide, Plastic Gull Wing Small Outline (SOIC)

Packaging Information

8P3, 8-Lead, 0.300" Wide,
Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-001 BA



8S2, 8-Lead, 0.200" Wide,
Plastic Gull Wing Small Outline (EIAJ SOIC)
Dimensions in Inches and (Millimeters)