

BIPOLAR ANALOG INTEGRATED CIRCUIT

μ PC1032H

030553

DUAL LOW NOISE PREAMPLIFIER

SILICON BIPOLAR MONOLITHIC INTEGRATED CIRCUIT

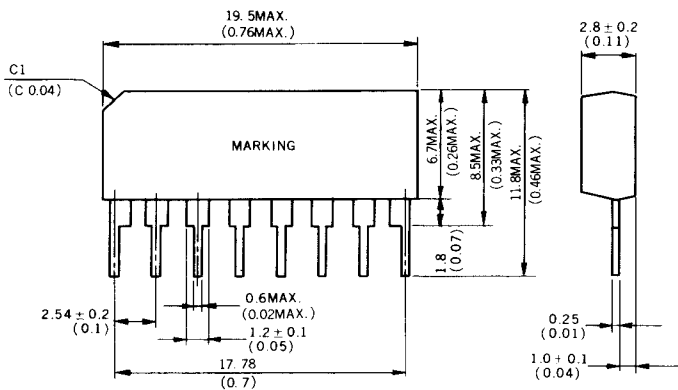
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DESCRIPTION

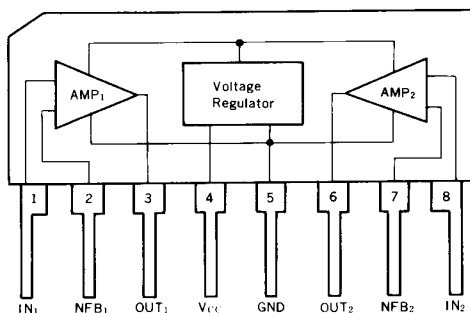
The μ PC1032H is a silicon monolithic integrated circuit designed for use as a 2 channel preamplifier for a car stereo set. The device has features of low noise, high gain, high output voltage and wide supply voltage range. Especially, as an advanced production process is used, the device has an excellent feature of very low pulsive noise. An internal voltage regulator circuit permits the μ PC1032H to operate satisfactorily over wide variation of supply voltage.

PACKAGE DIMENSIONS

in millimeters (inches)



CONNECTION DIAGRAM

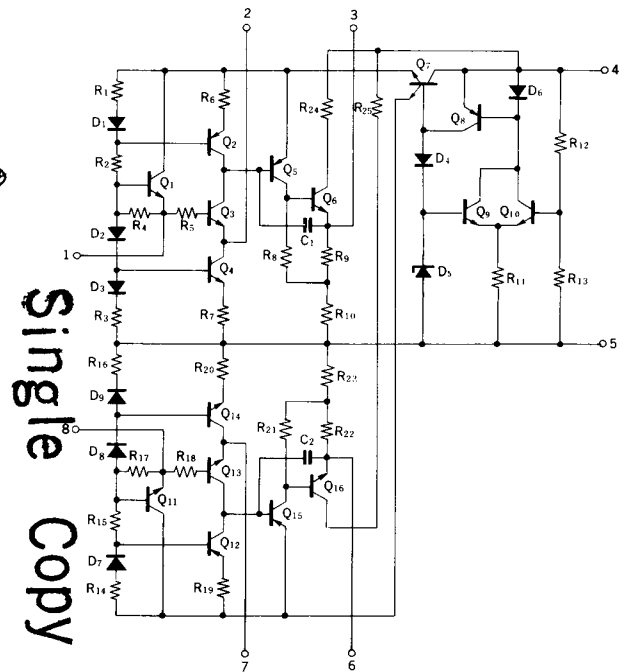


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FEATURES

- Two channel
- Wide supply voltage range
- Minimum number of external parts required
- Low noise, especially low pulsive noise
- SIP assures easy mounting on printed circuit board.

EQUIVALENT CIRCUIT



4.3
Handle With Care

Single Copy

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Nippon Electric Co., Ltd.

ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Supply Voltage	V _{CC}	18	V
Package Dissipation	P _D	270*	mW
Operating Temperature	T _{opt}	-20 to +75	°C
Storage Temperature	T _{stg}	-40 to +125	°C

*Ta = 75°C

RECOMMENDED CONDITIONS (Ta = 25°C)

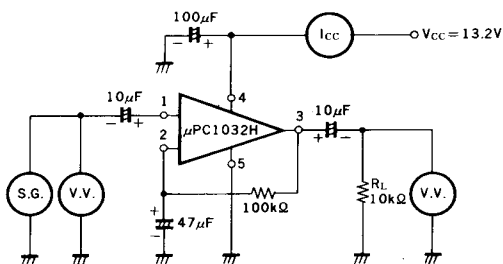
Operating Supply Voltage	V _{CC}	13.2	V
Supply Voltage Range	V _{CC}	8 to 17	V
Operating Ambient Temperature		-20 to +75	°C
Load impedance		10 kΩ TYP.	

ELECTRICAL CHARACTERISTICS (Ta = 25°C, V_{CC} = 13.2V, f = 1 kHz, R_L = 10 kΩ)

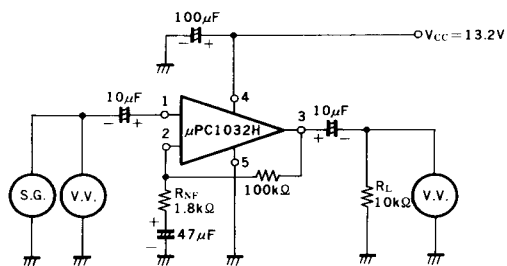
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CIRCUIT	TEST CONDITIONS
Circuit Current	I _{CC}		7	11.0	mA	①	v _{in} = 0
Open Loop Voltage Gain	A _{vo}	70	81		dB	①	v _o = 0.3V
Voltage Gain	A _v	33.5	35	35.5	dB	②	v _o = 0.3V, R _{NF} = 1.8 kΩ
Maximum Output Voltage	V _{OM}	1.1	1.7		V	③	T.H.D. = 1%, NAB ≅ 35 dB
Total Harmonic Distortion	T.H.D.		0.1	0.3	%	③	v _o = 0.3V, NAB ≅ 35 dB
Input Impedance	r _i	50	100		kΩ	③	
Equivalent Input Noise Voltage	v _{nin}		1.4	2.0	μVr.m.s.	④	R _G = 2.2kΩ, NAB ≅ 35dB
Cross Talk			-62		dB	⑤	v _o = 1V, (The other channel v _{in} = 0, R _G = 2.2kΩ)
Channel Balance		-0.3	0	+0.3	dB	⑤	v _o = 0.3V

TEST CIRCUITS

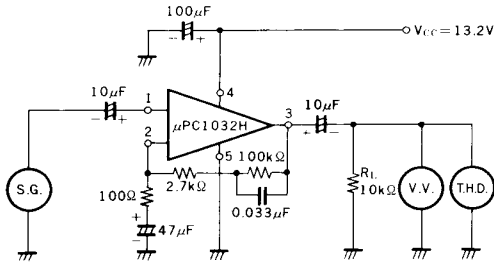
① I_{CC}, A_{vo} Test Circuit



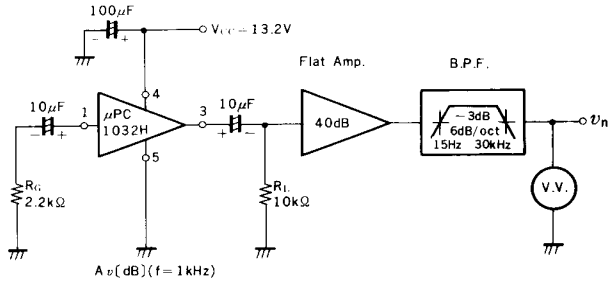
② A_v Test Circuit (for Ch. 1)



③ V_{OM} , T.H.D., r_i Test Circuit
(for Ch. 1)

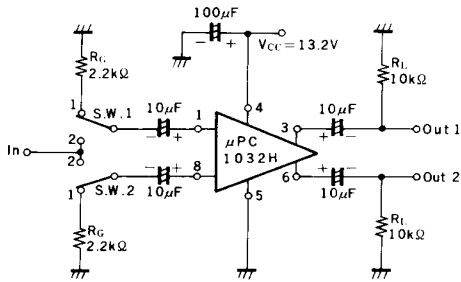


④ v_{nin} Test Circuit
(for Ch. 1)



v_{nin} is calculated by v_n and amp. gain ($A_v + 40$ dB).
External components of the IC are the same as the Test Circuit ③

⑤ Cross Talk, Channel Balance Test Circuit



External Components of the IC are the same as the Test Circuit ③

Cross talk Test Procedure

$$20 \log \text{Out}_2 / \text{Out}_1$$

Switch Position $SW_1 \rightarrow 2, SW_2 \rightarrow 1$

$$20 \log \text{Out}_1 / \text{Out}_2$$

Switch Position $SW_1 \rightarrow 1, SW_2 \rightarrow 2$

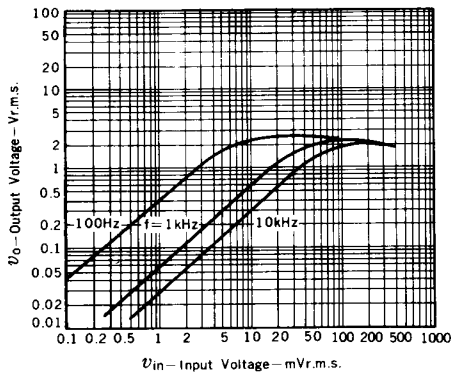
Channel Balance Test Procedure

$$20 \log \text{Out}_1 / \text{Out}_2$$

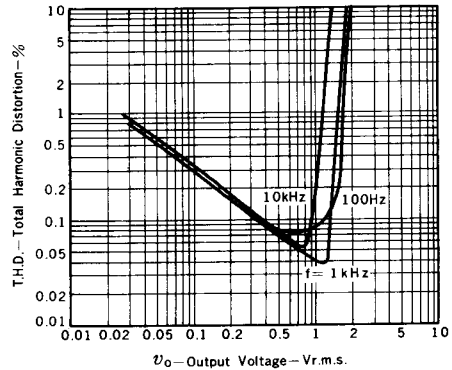
Switch Position $SW_1 \rightarrow 2, SW_2 \rightarrow 2$

TYPICAL CHARACTERISTICS ($T_a = 25^\circ\text{C}$)

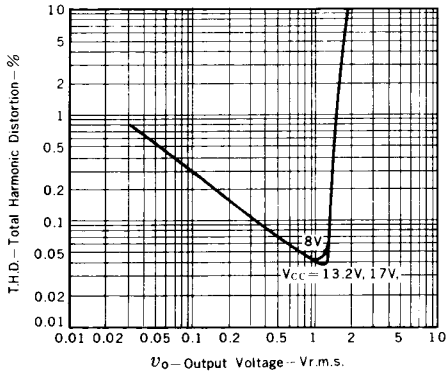
OUTPUT VOLTAGE vs. INPUT VOLTAGE
(Test Circuit ③)



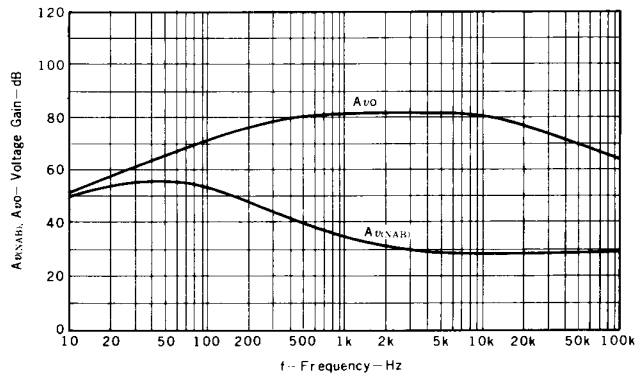
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE
(Test Circuit ③)



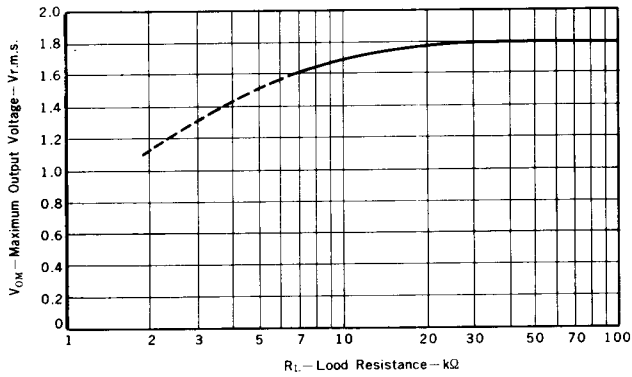
TOTAL HARMONIC DISTORTION vs. OUTPUT VOLTAGE
(Test Circuit 3)



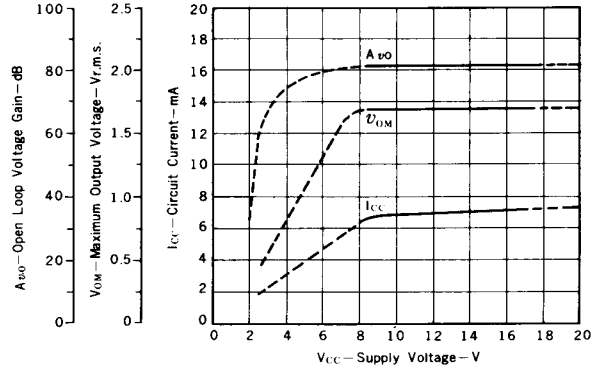
VOLTAGE GAIN vs. FREQUENCY
(Test Circuit 1, 3)



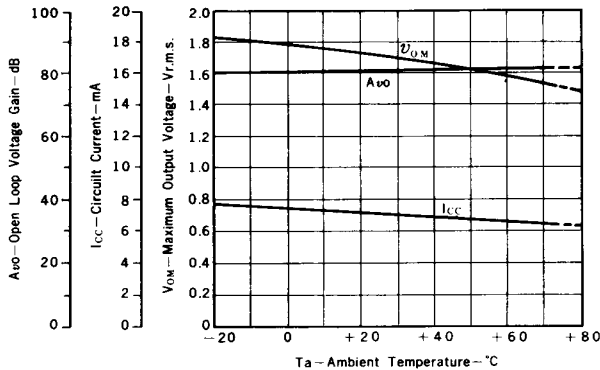
MAXIMUM OUTPUT VOLTAGE vs. LOAD RESISTANCE
(Test Circuit 3)



CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN vs. SUPPLY VOLTAGE
(Test Circuit 1, 3)

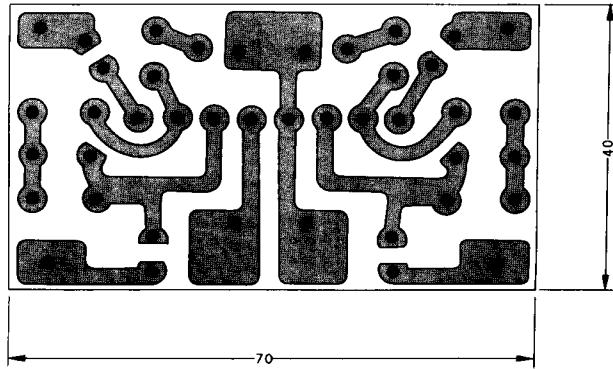


CIRCUIT CURRENT, MAXIMUM OUTPUT VOLTAGE, OPEN LOOP VOLTAGE GAIN AMBIENT TEMPERATURE
(Test Circuit 1, 3)

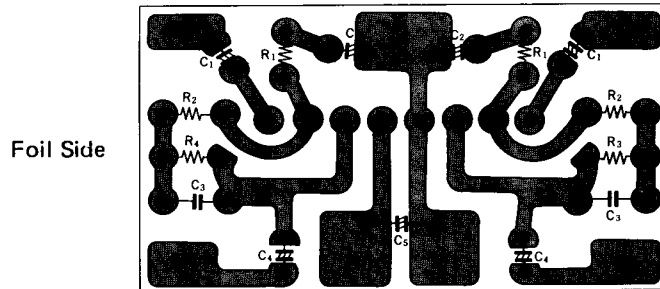


TYPICAL PRINTED CIRCUIT BOARD PATTERN

Bottom View (Unit : millimeters)



Components Layout



Components Side

