PALCE22V10 Family
24-Pin EE CMOS Versatile PAL Device

**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- As fast as 5-ns propagation delay and 142.8 MHz f_{MAX} (external)
- Low-power EE CMOS
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Peripheral Component Interconnect (PCI) compliant (-5/-7/-10)

- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP, 24-pin SOIC, 24-pin Flatpack and 28-pin PLCC and LCC packages save space
- 5-ns and 7.5-ns versions utilize split leadframes for improved performance

GENERAL DESCRIPTION

The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.
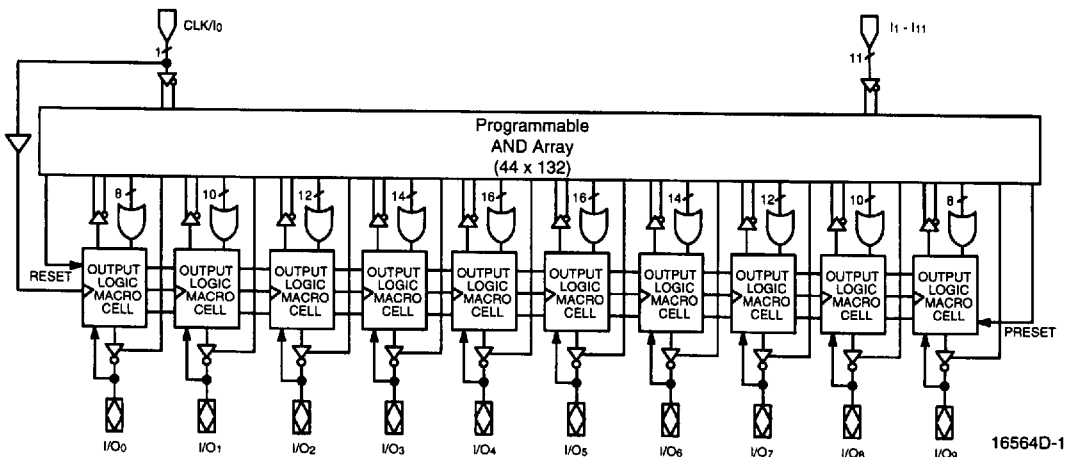
The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to 16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active

high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.
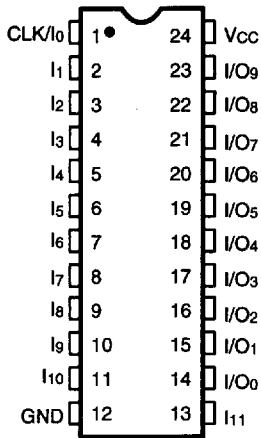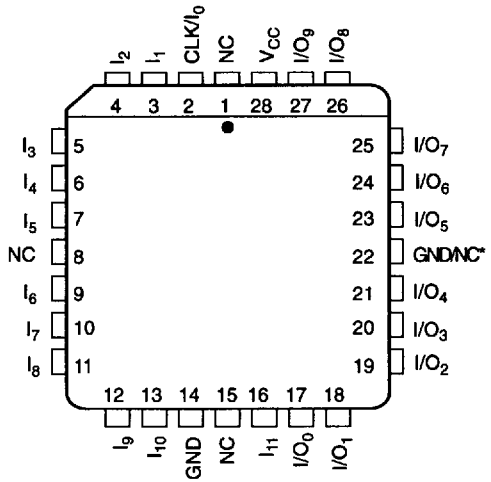
BLOCK DIAGRAM

16564D-1

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2-217

CONNECTION DIAGRAMS

Top View

SKINNYDIP/SOIC/FLATPACK

CLK/I_0	1 ●	24	V_{CC}
I_1	2	23	I/O_9
I_2	3	22	I/O_8
I_3	4	21	I/O_7
I_4	5	20	I/O_6
I_5	6	19	I/O_5
I_6	7	18	I/O_4
I_7	8	17	I/O_3
I_8	9	16	I/O_2
I_9	10	15	I/O_1
I_{10}	11	14	I/O_0
GND	12	13	I_{11}

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PLCC/LCC

Top pins (left to right): I_2 (4), I_1 (3), CLK/I_0 (2), NC (1), V_{CC} (28), I/O_9 (27), I/O_8 (26)

Left side (top to bottom): I_3 (5), I_4 (6), I_5 (7), NC (8), I_6 (9), I_7 (10), I_8 (11)

Bottom pins (left to right): I_9 (12), I_{10} (13), GND (14), NC (15), I_{11} (16), I/O_0 (17), I/O_1 (18)

Right side (top to bottom): I/O_7 (25), I/O_6 (24), I/O_5 (23), GND/NC* (22), I/O_4 (21), I/O_3 (20), I/O_2 (19)

16564D-3

* For -5, this pin must be grounded for guaranteed data sheet performance. If not grounded, AC timing may degrade by about 10%.
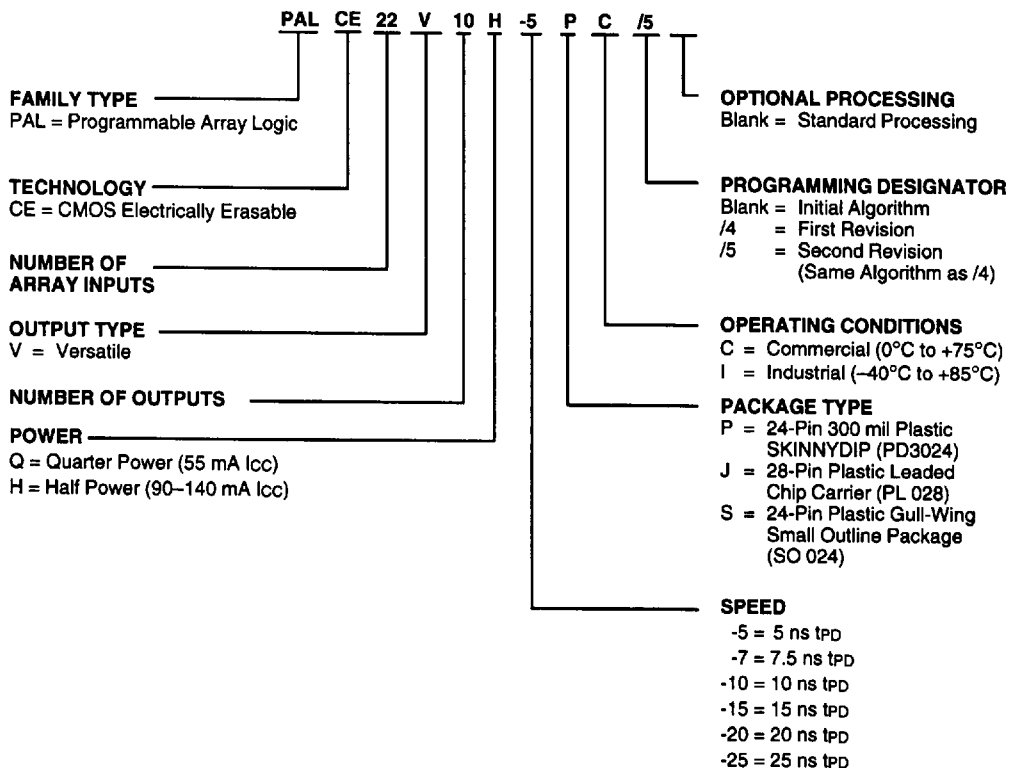
Note:
Pin 1 is marked for orientation.

PIN DESIGNATIONS

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

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PAL  CE  22  V  10  H  -5  P  C  /5
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FAMILY TYPE
PAL = Programmable Array Logic

TECHNOLOGY
CE = CMOS Electrically Erasable

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF OUTPUTS

POWER
Q = Quarter Power (55 mA Icc)
H = Half Power (90–140 mA Icc)

OPTIONAL PROCESSING
Blank = Standard Processing

PROGRAMMING DESIGNATOR
Blank = Initial Algorithm
/4 = First Revision
/5 = Second Revision
(Same Algorithm as /4)

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
P = 24-Pin 300 mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL028)
S = 24-Pin Plastic Gull-Wing Small Outline Package (SO 024)

SPEED
-5 = 5 ns t_{PD}
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}
-25 = 25 ns t_{PD}

Valid Combinations		
PALCE22V10-5	JC	
PALCE22V10H-7	PC, JC	/5
PALCE22V10H-10	PC, JC, SC, PI, JI, ZC	
PALCE22V10Q-10	PC, JC	
PALCE22V10H-15	PC, JC, PI, JI, ZC	Blank, /5, /4
PALCE22V10Q-15	PC, JC	/5
PALCE22V10H-20	PI, JI	/4
PALCE22V10H-25	PC, JC, SC, PI, JI	Blank, /4
PALCE22V10Q-25	PC, JC	

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.
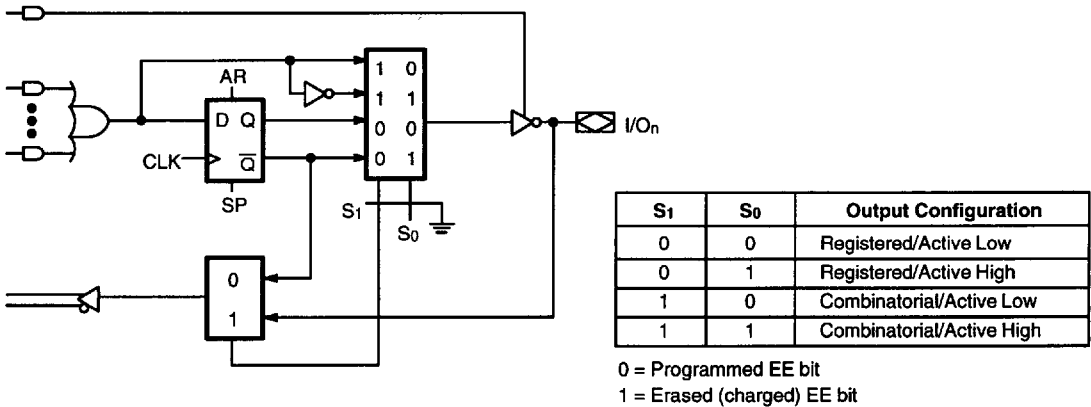

S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

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Figure 1. Output Logic Macrocell Diagram

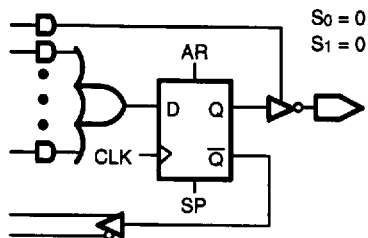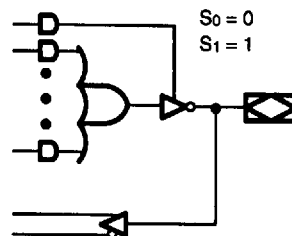## Registered Output Configuration

Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.
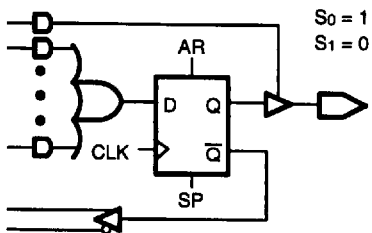
Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

Registered/Active Low

Combinatorial/Active Low

Registered/Active High
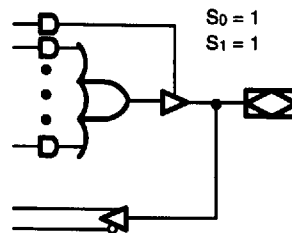
Combinatorial/Active High

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Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The V_{CC} rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE22V10 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

PCI Compliance

The PALCE22V10H-5/7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE22V10H-5/7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design.

LOGIC DIAGRAM
SKINNYDIP/SOIC/FLATPACK (PLCC/LCC) Pinouts
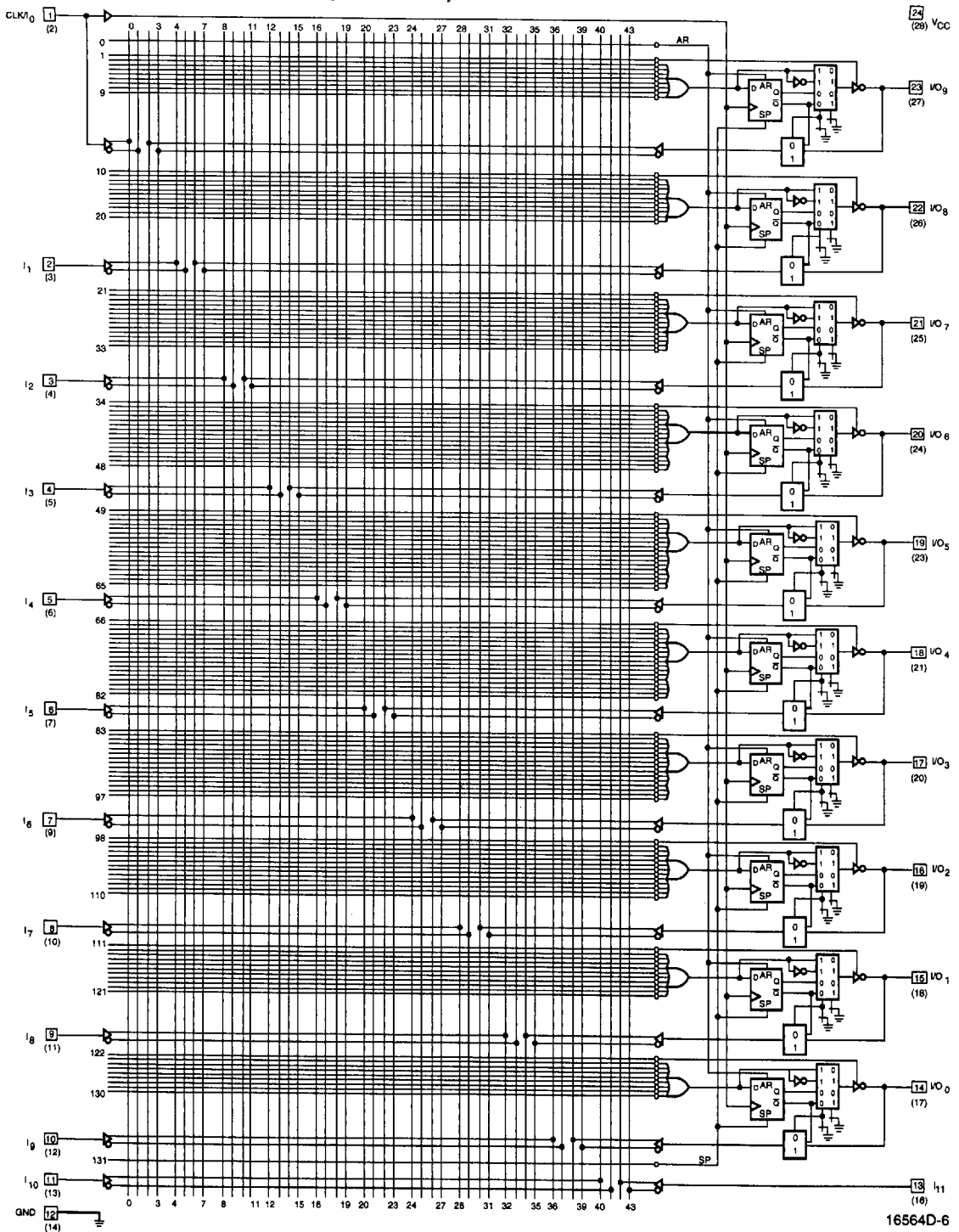
16564D-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin
Voltage .... −0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage .... 2001 V

Latchup Current (T_A = 0°C to +75°C) ...... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air .... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground .... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)	−30	−130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		125	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

■ 0257526 0036829 030 ■

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	$T_A = 25°C$ $f = 1$ MHz	8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-5 Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				5	ns
t_{S1}	Setup Time from Input or Feedback			3		ns
t_{S2}	Setup Time from SP to Clock			4		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				4	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				0.5	ns
t_{AR}	Asynchronous Reset to Registered Output				7.5	ns
t_{ARW}	Asynchronous Reset Width			4.5		ns
t_{ARR}	Asynchronous Reset Recovery Time			4.5		ns
t_{SPR}	Synchronous Preset Recovery Time			4.5		ns
t_{WL}	Clock Width	LOW		2.5		ns
t_{WH}		HIGH		2.5		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	142.8		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 5)	150		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	200		MHz
t_{EA}	Input to Output Enable Using Product Term Control				6	ns
t_{ER}	Input to Output Disable Using Product Term Control				5.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*

3. *Skew is measured with all outputs switching in the same direction.*

4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

5. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) − t_S.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin
Voltage .... −0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage .... 2001 V

Latchup Current (T_A = 0°C to +75°C) ...... 100 mA

*Stresses above those listed under Absolute Maximum Ratings
may cause permanent device failure. Functionality at or above
these limits is not implied. Exposure to absolute maximum rat-
ings for extended periods may affect device reliability.*

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air .... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground .... +4.75 V to +5.25 V

*Operating Ranges define those limits between which the func-
tionality of the device is guaranteed.*

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25°C (Note 3)	−30	−130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.*
   V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C$_{IN}$	Input Capacitance	V$_{IN}$ = 2.0 V	V$_{CC}$ = 5.0 V T$_A$ = 25°C f = 1 MHz	5	pF
C$_{OUT}$	Output Capacitance	V$_{OUT}$ = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7 PDIP Min	-7 PDIP Max	-7 PLCC Min	-7 PLCC Max	Unit
t$_{PD}$	Input or Feedback to Combinatorial Output			3	7.5	3	7.5	ns
t$_{S1}$	Setup Time from Input or Feedback			5		4.5		ns
t$_{S2}$	Setup Time from SP to Clock			6		6		ns
t$_H$	Hold Time			0		0		ns
t$_{CO}$	Clock to Output			2	5	2	4.5	ns
t$_{SKEWR}$	Skew Between Registered Outputs (Note 3)				1		1	ns
t$_{AR}$	Asynchronous Reset to Registered Output				10		10	ns
t$_{ARW}$	Asynchronous Reset Width			7		7		ns
t$_{ARR}$	Asynchronous Reset Recovery Time			7		7		ns
t$_{SPR}$	Synchronous Preset Recovery Time			7		7		ns
t$_{WL}$	Clock Width	LOW		3.5		3.0		ns
t$_{WH}$		HIGH		3.5		3.0		ns
f$_{MAX}$	Maximum Frequency (Note 4)	External Feedback	1/(ts + tco)	100		111		MHz
		Internal Feedback (fCNT)	1/(ts + tCF) (Note 5)	125		133		MHz
		No Feedback	1/(twH + twL)	142.8		166		MHz
t$_{EA}$	Input to Output Enable Using Product Term Control				7.5		7.5	ns
t$_{ER}$	Input to Output Disable Using Product Term Control				7.5		7.5	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. Skew is measured with all outputs switching in the same direction.

4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

5. tCF is a calculated value and is not guaranteed. tCF can be found using the following equation:
tCF = 1/fMAX (internal feedback) − ts.

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Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to Vcc + 1.0 V

DC Output or I/O Pin
Voltage .... −0.5 V to Vcc + 1.0 V

Static Discharge Voltage .... 2001 V

Latchup Current (TA = 0°C to +75°C) ...... 100 mA

*Stresses above those listed under Absolute Maximum Ratings
may cause permanent device failure. Functionality at or above
these limits is not implied. Exposure to absolute maximum rat-
ings for extended periods may affect device reliability.*

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air .... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground .... +4.75 V to +5.25 V

*Operating Ranges define those limits between which the func-
tionality of the device is guaranteed.*

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

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V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25° C (Note 3)	−30	−130	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		120	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.*
   V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V	5	
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	$T_A = 25°C$ $f = 1$ MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_{S1}	Setup Time from Input or Feedback			6		ns
t_{S2}	Setup Time from SP to Clock			7		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

4. t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:
$t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with
Power Applied . . . . −55°C to +125°C

Supply Voltage with Respect
to Ground . . . . −0.5 V to +7.0 V

DC Input Voltage . . . . −0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin
Voltage . . . . −0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage . . . . 2001 V

Latchup Current (T_A = 0°C to +75°C) . . . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES
Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	−30	−130	mA
I_{CC} (Static)	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max (Note 4)		55	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

4. *This parameter is guaranteed worst case under test condition. Refer to the I_{CC} vs. frequency graph for typical I_{CC} characteristics.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V $T_A = 25°C$ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10 Min	-10 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				10	ns
t_S	Setup Time from Input, Feedback or SP to Clock			6		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				6	ns
t_{AR}	Asynchronous Reset to Registered Output				13	ns
t_{ARW}	Asynchronous Reset Width			8		ns
t_{ARR}	Asynchronous Reset Recovery Time			8		ns
t_{SPR}	Synchronous Preset Recovery Time			8		ns
t_{WL}	Clock Width	LOW		4		ns
t_{WH}		HIGH		4		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	83		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CO})$ (Note 4)	110		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	125		MHz
t_{EA}	Input to Output Enable Using Product Term Control				10	ns
t_{ER}	Input to Output Disable Using Product Term Control				9	ns

Notes:

2. *See Switching Test Circuit for test conditions.*

3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
   $t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin
Voltage .... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage .... 2001 V

Latchup Current (T_A = 0°C to +75°C) ...... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air .... 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground (H/Q-15) .... +4.75 V to +5.25 V

Supply Voltage (V_{CC}) with
Respect to Ground (H/Q-25) ...... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			−100	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			−100	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)		−30	−130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second.*
   V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V $T_A = 25°C$	5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	$f = 1$ MHz	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15		-25		Unit
				Min	Max	Min	Max	
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	$1/(t_S + t_{CO})$	50		33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$ (Note 4)	58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
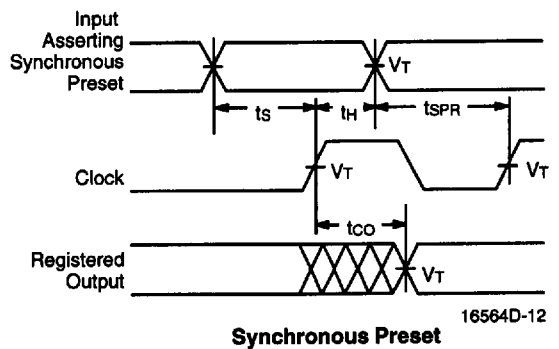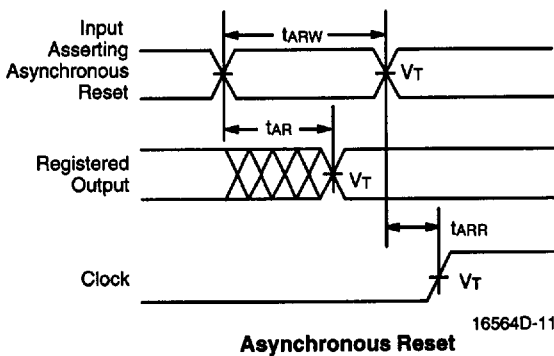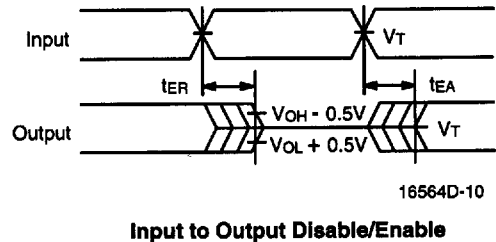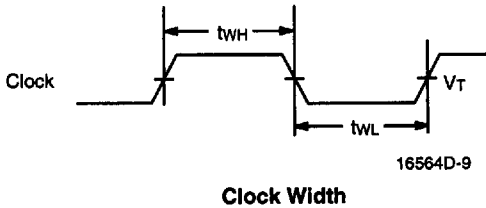
4. t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:
$t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin
Voltage .... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage .... 2001 V

Latchup Current (T_A = −40°C to +85°C) .... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air .... −40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground .... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description		Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage		I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage		I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage		Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage		Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current		V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	μA
I_{IL}	Input LOW Leakage Current		V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	μA
I_{OZH}	Off-State Output Leakage Current HIGH		V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	μA
I_{OZL}	Off-State Output Leakage Current LOW		V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	μA
I_{SC}	Output Short-Circuit Current		V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)	−30	−130	mA
I_{CC} (Static)	Supply Current	H-20/25	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max		100	mA
		H-10/15			110	
I_{CC} (Dynamic)	Supply Current		V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max, f = 15 MHz		130	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*

2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*

3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

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CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	$V_{IN} = 2.0$ V	$V_{CC} = 5.0$ V $T_A = 25°C$	5	
C_{OUT}	Output Capacitance	$V_{OUT} = 2.0$ V	$f = 1$ MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-10		-15		-20		-25		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
tPD	Input or Feedback to Combinatorial Output				10		15		20		25	ns
ts	Setup Time from Input, Feedback or SP to Clock			7		10		12		15		ns
tH	Hold Time			0		0		0		0		ns
tco	Clock to Output				6		10		12		15	ns
tAR	Asynchronous Reset to Registered Output				13		20		25		25	ns
tARW	Asynchronous Reset Width			8		15		20		25		ns
tARR	Asynchronous Reset Recovery Time			8		10		20		25		ns
tSPR	Synchronous Preset Recovery Time8					10		14		25		ns
tWL	Clock Width	LOW		4		8		10		13		ns
tWH		HIGH		4		8		10		13		ns
fMAX	Maximum Frequency (Note 3)	External Feedback	1/(ts + tco)	83.3		50		41.6		33.3		MHz
		Internal Feedback (fCNT)	1/(ts + tCF) (Note 4)	110		58.8		45.4		35.7		MHz
		No Feedback	1/(tWH + tWL)	125		83.3		50		38.5		MHz
tEA	Input to Output Enable Using Product Term Control				10		15		20		25	ns
tER	Input to Output Disable Using Product Term Control				9		15		20		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*

3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
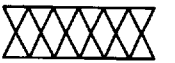 $t_{CF} = 1/f_{MAX}$ *(internal feedback)* $- t_S$.

SWITCHING WAVEFORMS

16564D-7

Combinatorial Output

16564D-8

Registered Output

16564D-9

Clock Width

16564D-10

Input to Output Disable/Enable

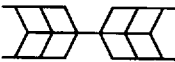16564D-11

Asynchronous Reset

16564D-12
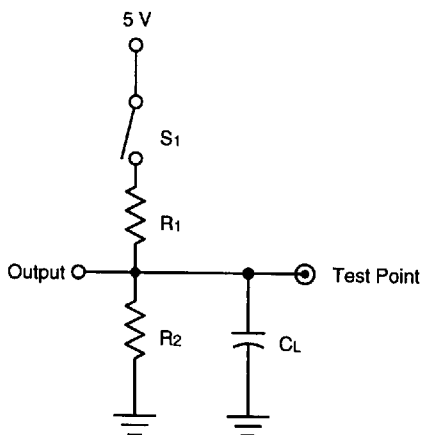
Synchronous Preset

Notes:

1. $V_T = 1.5$ V.

2. Input pulse amplitude 0 V to 3.0 V.

3. Input rise and fall times 2 ns – 5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
———	Must be Steady	Will be Steady
(falling hatched)	May Change from H to L	Will be Changing from H to L
(rising hatched)	May Change from L to H	Will be Changing from L to H
XXXXXX	Don't Care, Any Change Permitted	Changing, State Unknown
⟩⟩⟩—⟨⟨⟨	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

16564D-13

Specification	S₁	C_L	Commercial		Measured Output Value
			R₁	R₂	
t_PD, t_CO	Closed			All except H-5/7:	1.5 V
t_EA	Z → H: Open Z → L: Closed	50 pF	300 Ω	390 Ω	1.5 V
t_ER	H → Z: Open L → Z: Closed	5 pF		H-5/7: 300 Ω	H → Z: V_OH − 0.5 V L → Z: V_OL + 0.5 V

TYPICAL I_CC CHARACTERISTICS
$V_{CC} = 5.0$ V, $T_A = 25°C$
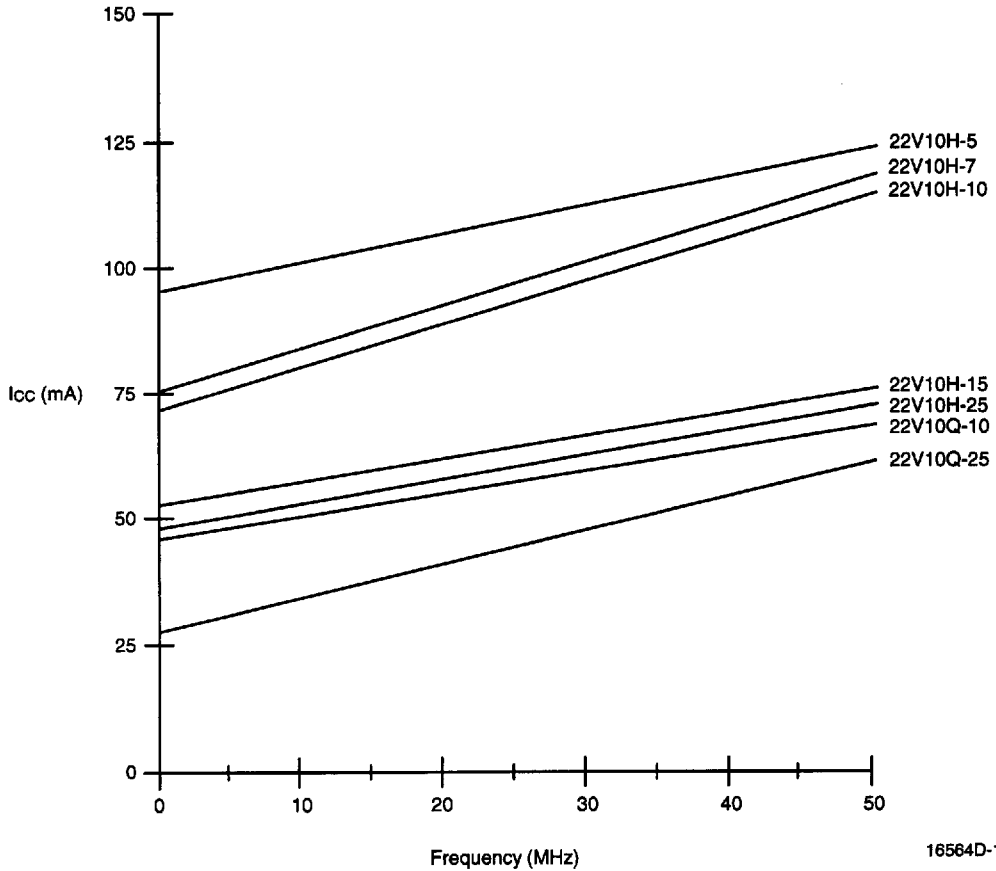
I_CC vs. Frequency

16564D-14

The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.

By utilizing 50% of the device, a midpoint is defined for I_CC. From this midpoint, a designer may scale the I_CC graphs up or down to estimate the I_CC requirements for a particular design.

ENDURANCE CHARACTERISTICS

The PALCE22V10 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Endurance Characteristics

Symbol	Parameter	Test Conditions	Min	Unit
tDR	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

Bus-Friendly Inputs

The PALCE22V10H-15/25, Q-25 (Com'l) and H-20 (Ind) inputs and I/O loop back to the input after the second stage of the input buffer. This configuration reinforces the state of the input and pulls the voltage away from the input threshold voltage. Unlike a pull-up, this configuration cannot cause contention on a bus. For an illustration of this configuration, see the input/output equivalent schematics.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR SELECTED /4 DEVICES*
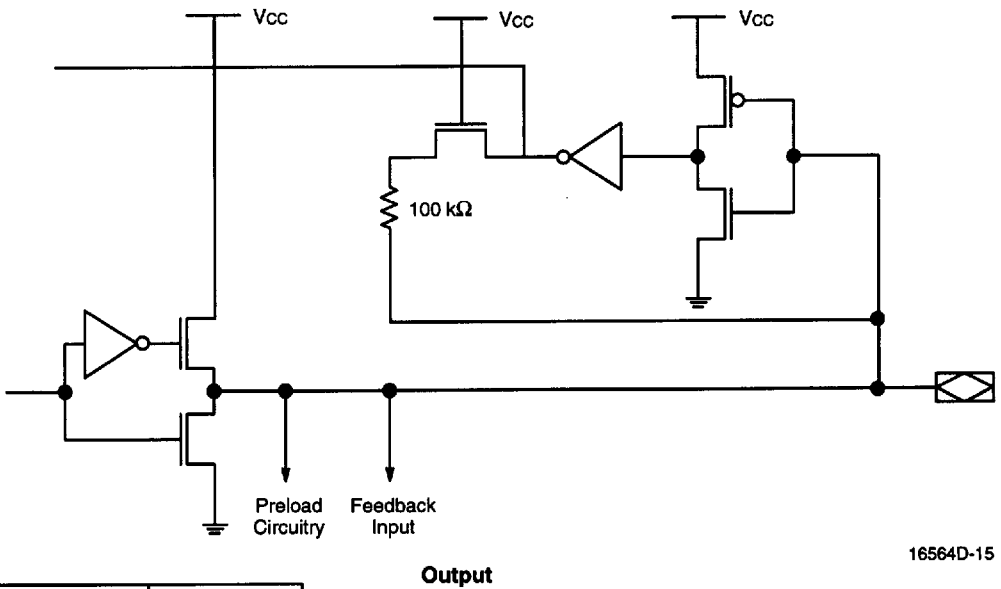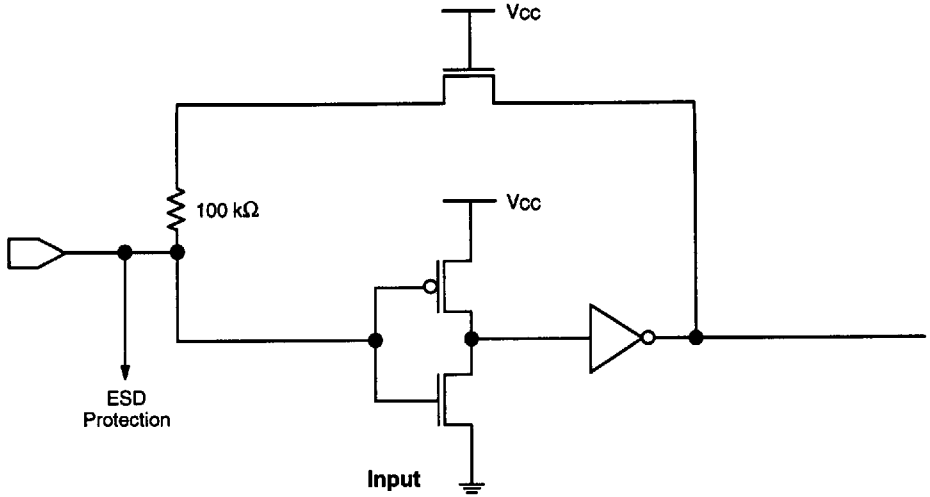
16564D-15

Device	Rev Letter
PALCE22V10H-15	
PALCE22V10H-20	H
PALCE22V10H-25	
PALCE22V10Q-25	I

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ROBUSTNESS FEATURES

The PALCE22V10X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 version. Selected /4 devices are also being retrofitted with these robustness features. See the chart below for device listing.

INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSION AND SELECTED /4 DEVICES*
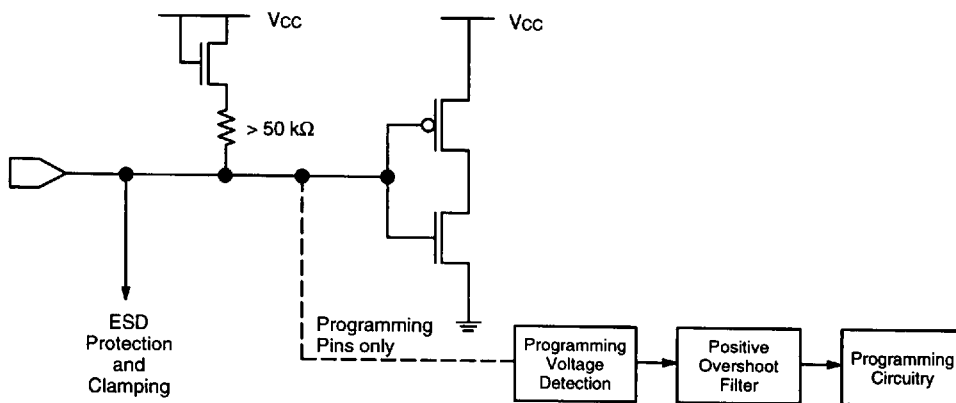
Typical Input
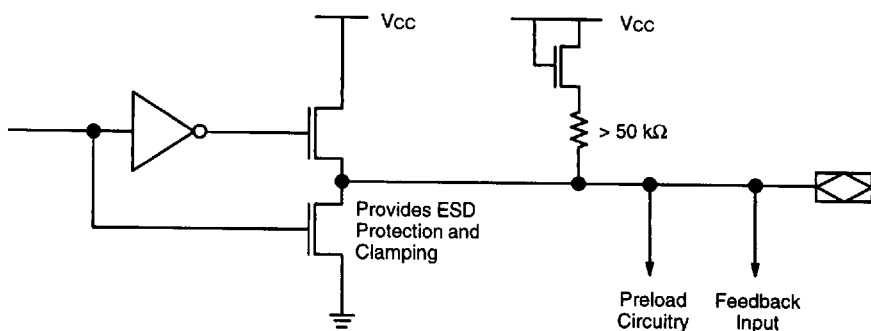
16564D-16

Typical Output

Device	Rev Letter
PALCE22V10H-15	D
PALCE22V10H-25	D
PALCE22V10Q-25	F

Topside Marking:
AMD CMOS PLD's are marked on top of the package in the following manner:
PALCEXXXX
Datecode (3 numbers) Lot ID (4 characters)– –(Rev Letter)
The Lot ID and Rev Letter are separated by two spaces.

0257526 0036846 11T

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways

V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

■ The V_{CC} rise must be monotonic.

■ Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max	Unit
t_{PR}	Power-up Reset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		
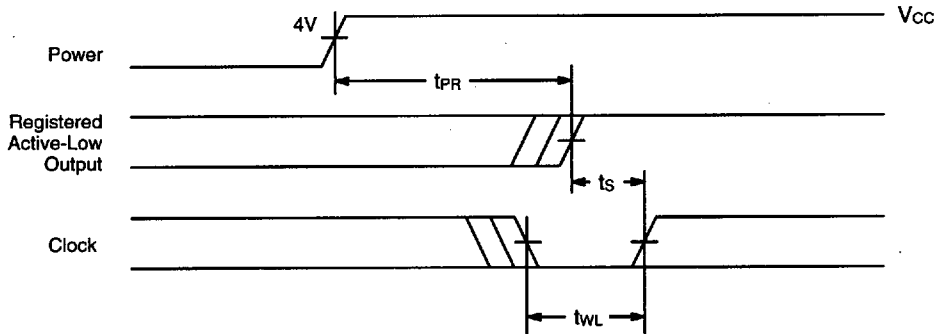
Power-Up Reset Waveform

TYPICAL THERMAL CHARACTERISTICS
PALCE22V10/4 (PALCE22V10H-15)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θjc	Thermal impedance, junction to case		15	16	°C/W
θja	Thermal impedance, junction to ambient		72	54	°C/W
θjma	Thermal impedance, junction to ambient with air flow	200 lfpm air	67	49	°C/W
		400 lfpm air	60	43	°C/W
		600 lfpm air	53	37	°C/W
		800 lfpm air	46	31	°C/W

PALCE22V10/5 (PALCE22V10H-10)

Measured at 25°C ambient. These parameters are not tested.

Parameter Symbol	Parameter Description		Typ		Unit
			SKINNYDIP	PLCC	
θjc	Thermal impedance, junction to case		20	18	°C/W
θja	Thermal impedance, junction to ambient		73	55	°C/W
θjma	Thermal impedance, junction to ambient with air flow	200 lfpm air	66	48	°C/W
		400 lfpm air	61	43	°C/W
		600 lfpm air	55	40	°C/W
		800 lfpm air	52	37	°C/W

Plastic θjc Considerations

The data listed for plastic θjc are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the θjc measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, θjc tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.

PALCE22V10Z Family

Zero-Power 24-Pin EE CMOS Versatile PAL Device

**Advanced
Micro
Devices**

DISTINCTIVE CHARACTERISTICS

- ■ **Zero-power CMOS technology**
  - — 30 µA standby current
  - — As fast as 15 ns first-access propagation delay and 50 MHz f$_{MAX}$ (external)
- ■ **Unused product term disable for reduced power consumption**
- ■ **Available in Industrial operating range at 15 ns t$_{PD}$**
  - — T$_A$ = –40°C to +85°C
  - — V$_{CC}$ = +4.5 V to +5.5 V
- ■ **HC- and HCT-compatible inputs and outputs**
- ■ **Electrically-erasable technology provides reconfigurable logic and full testability**

- ■ **10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs**
- ■ **Varied product term distribution allows up to 16 product terms per output for complex functions**
- ■ **Global asynchronous reset and synchronous preset for initialization**
- ■ **Power-up reset for initialization and register preload for testability**
- ■ **Extensive third-party software and programmer support through FusionPLD partners**
- ■ **24-pin SKINNYDIP, 28-pin PLCC, and 24-pin SOIC packages save space**

GENERAL DESCRIPTION

The PALCE22V10Z is an advanced PAL device built with zero-power, high-speed, electrically-erasable CMOS technology. It provides user-programmable logic for replacing conventional zero-power CMOS SSI/MSI gates and flip-flops at a reduced chip count.

The PALCE22V10Z provides zero standby power and high speed. At 30 µA maximum standby current, the PALCE22V10Z allows battery powered operation for an extended period.

The ZPAL™ device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds

the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10Z designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the Software Reference Guide to PLD Compliers for certified development systems, and the Programmer Reference Guide for approved programmers.
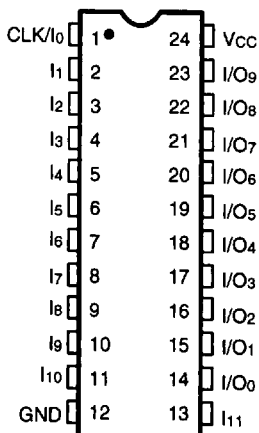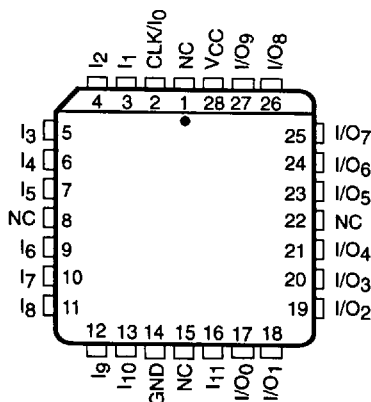
BLOCK DIAGRAM
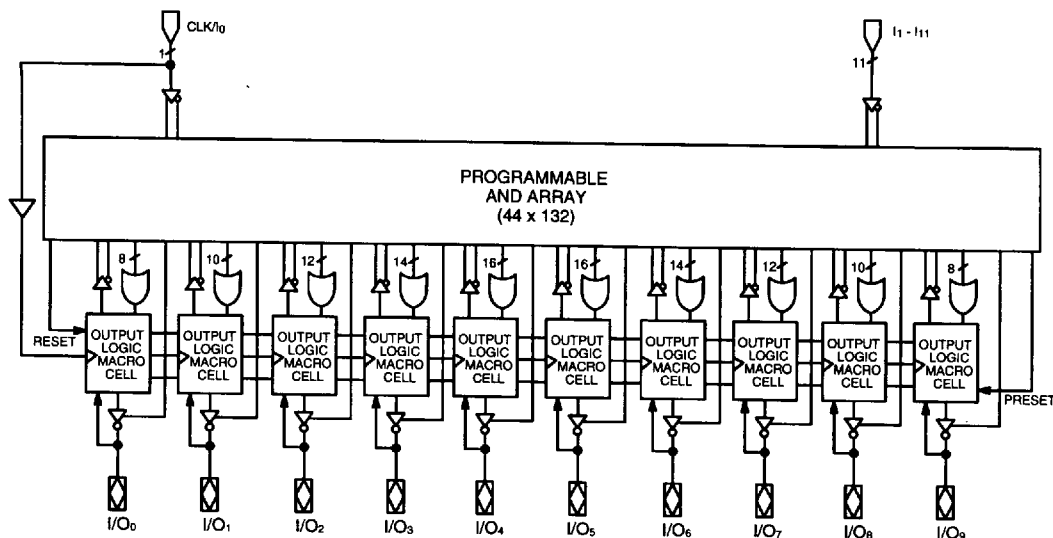
15700E-1

CONNECTION DIAGRAMS

Top View

SKINNYDIP/SOIC

15700E-2

PLCC

15700E-3

Note:

Pin 1 is marked for orientation.

PIN DESCRIPTION
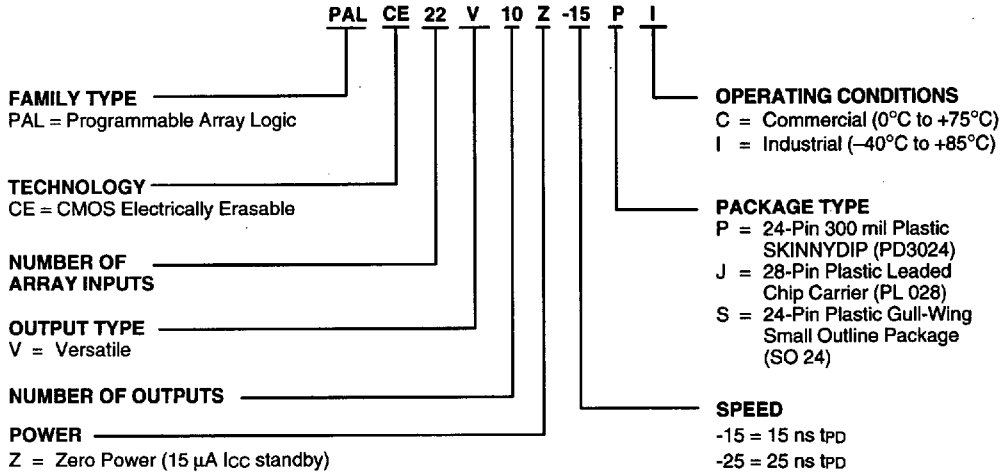
CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of these elements:

PAL CE 22 V 10 Z -15 P I

FAMILY TYPE
PAL = Programmable Array Logic

TECHNOLOGY
CE = CMOS Electrically Erasable

NUMBER OF ARRAY INPUTS

OUTPUT TYPE
V = Versatile

NUMBER OF OUTPUTS

POWER
Z = Zero Power (15 μA I_{CC} standby)

OPERATING CONDITIONS
C = Commercial (0°C to +75°C)
I = Industrial (−40°C to +85°C)

PACKAGE TYPE
P = 24-Pin 300 mil Plastic SKINNYDIP (PD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
S = 24-Pin Plastic Gull-Wing Small Outline Package (SO 24)

SPEED
-15 = 15 ns t_{PD}
-25 = 25 ns t_{PD}

Valid Combinations	
PALCE22V10Z-15	PI, JI
PALCE22V10Z-25	PC, JC, SC, PI, JI, SI

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

The PALCE22V10Z is the zero-power version of the PALCE22V10. It has all the architectural features of the PALCE22V10. In addition, the PALCE22V10Z has zero standby power and unused product term disable.

The PALCE22V10Z allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10Z has 12 inputs and 10 I/O macrocells. The macrocell (Figure 1) allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 2). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits $S_0 - S_1$. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it floats to V_{CC} (1), selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

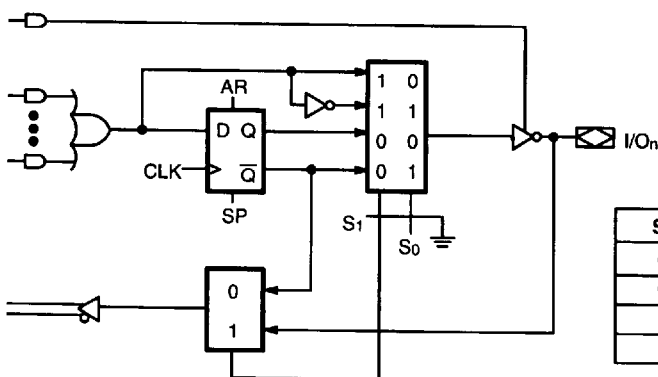## Variable Input/Output Pin Ratio

The PALCE22V10Z has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.

Registered Output Configuration

Each macrocell of the PALCE22V10Z includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.
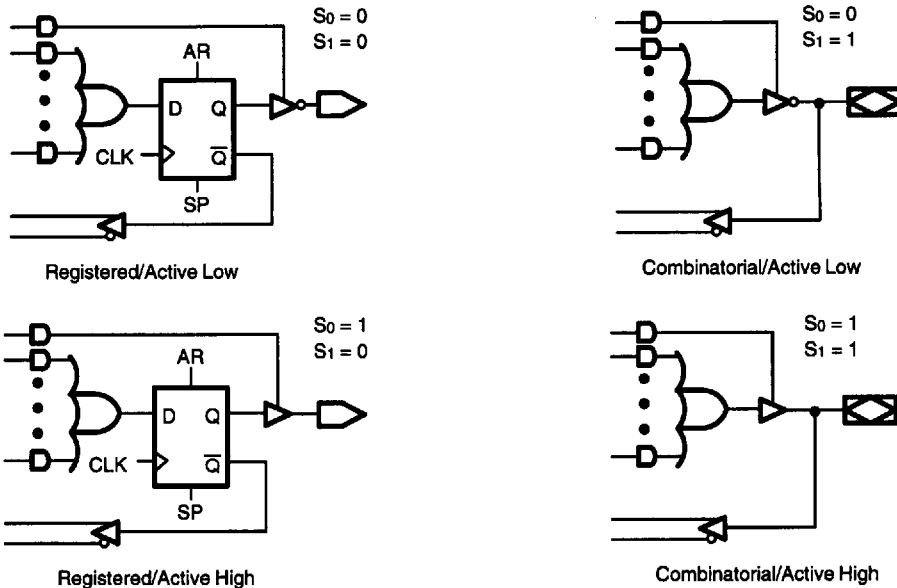

S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

15700E-4

Figure 1. Output Logic Macrocell

Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10Z has additional Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Zero-Standby Power Mode

The PALCE22V10Z features a zero-standby power mode. When none of the inputs switch for an extended period (typically 50 ns), the PALCE22V10Z will go into standby mode, shutting down most of its internal circuitry. The current will go to almost zero ($I_{CC} < 30$ μA). The outputs will maintain the states held before the device went into the standby mode.

When any input switches, the internal circuitry is fully enabled and power consumption returns to normal. This feature results in considerable power savings for operation at low to medium frequencies. This savings is illustrated in the Icc vs. frequency graph.

Product-Term Disable

On a programmed PALCE22V10Z, any product terms that are not used are disabled. Power is cut off from these product terms so that they do not draw current. As shown in the Icc vs. frequency graph, product-term disabling results in considerable power savings. This savings is greater at the higher frequencies.

Further hints on minimizing power consumption can be found in the Application Note "Minimizing Power Consumption with Zero-Power PLDs."

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10Z will depend on the programmed output polarity. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The registers on the PALCE22V10Z can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10Z design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10Z can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

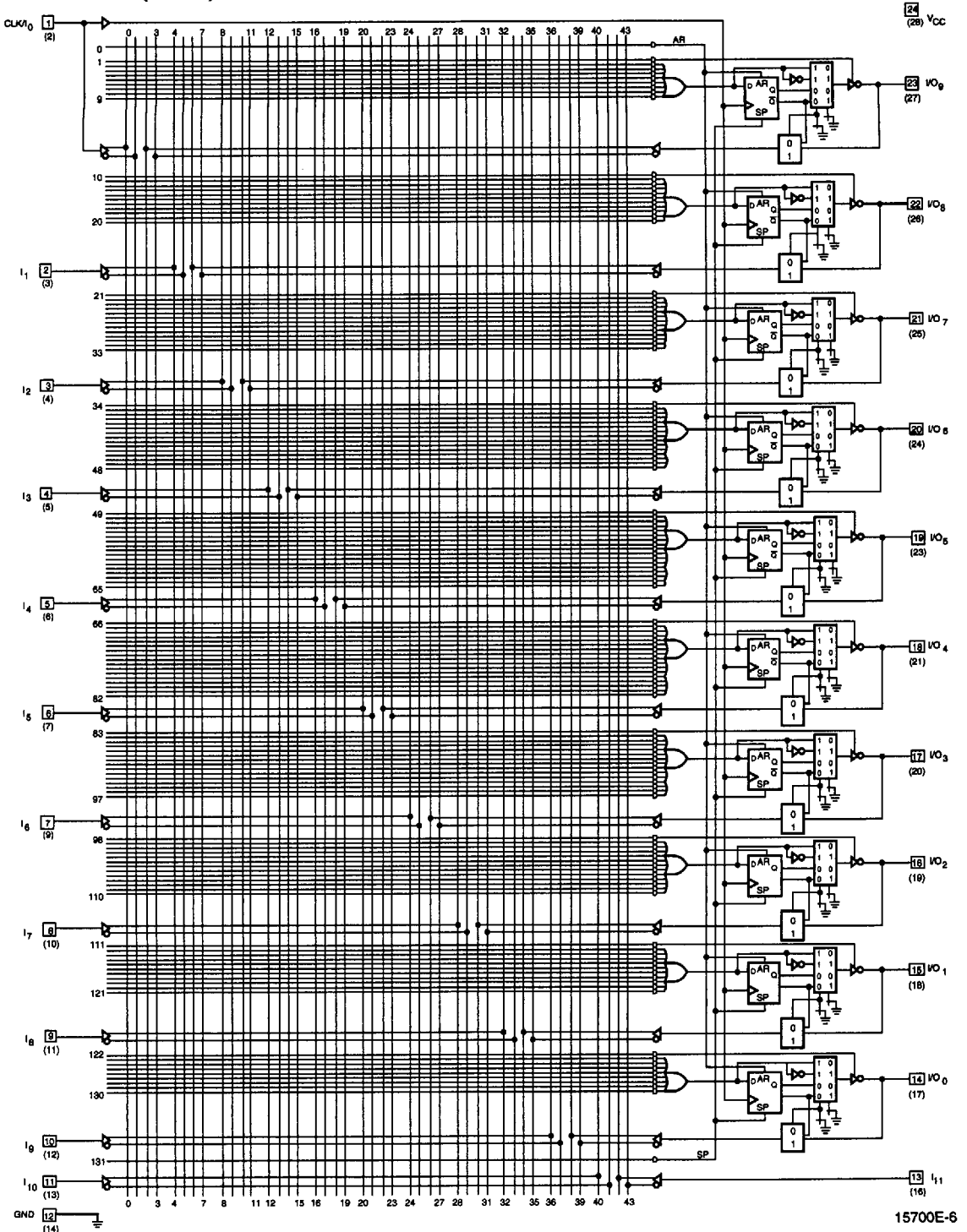The PALCE22V10Z offers a very high level of built-in quality.

The erasability of the CMOS PALCE22V10Z allows direct testing of the device array to guarantee 100% programming and functional yields.

Technology

The high-speed PALCE22V10Z is fabricated with AMD's advanced electrically-erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with HC and HCT devices. This technology provides strong input-clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

LOGIC DIAGRAM
SKINNYDIP (PLCC) Pinouts

15700E-6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature .... −65°C to +150°C

Ambient Temperature with
Power Applied .... −55°C to +125°C

Supply Voltage with Respect
to Ground .... −0.5 V to +7.0 V

DC Input Voltage .... −0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin
Voltage .... −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage .... 2001 V

Latchup Current (T_C = −40°C to +85°C) .... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Industrial (I) Devices

Operating Case
Temperature (T_C) .... −40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground .... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 μA	V_{CC}−0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 μA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	μA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			−10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			−10	μA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		−5	−150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		30	μA
		V_{CC} = Max	f = 15 MHz		100	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				10	ns
t_{AR}	Asynchronous Reset to Registered Output				20	ns
t_{ARW}	Asynchronous Reset Width			15		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		ns
t_{SPR}	Synchronous Preset Recovery Time			10		ns
t_{WL}	Clock Width	LOW		8		ns
t_{WH}		HIGH		8		ns
f_{MAX}	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_S + t_{CO})$	50		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	58.8		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15	ns
t_{ER}	Input to Output Disable Using Product Term Control				15	ns

Notes:

2. *See Switching Test Circuit for test conditions.*

3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*

4. *t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:*
$t_{CF} = 1/f_{MAX}$ *(internal feedback)* $- t_S$.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . −65°C to +150°C

Ambient Temperature with
Power Applied . . . . −55°C to +125°C

Supply Voltage with Respect
to Ground . . . . −0.5 V to +7.0 V

DC Input Voltage . . . . −0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin
Voltage . . . . −0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . 2001 V

Latchup Current (T_C = −40°C to +85°C) . . . . 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . 0°C to +75°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Operating Case
Temperature (T_C) . . . . −40°C to +85°C

Supply Voltage (V_{CC}) with
Respect to Ground . . . . +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = 6 mA	3.84		V
		V_{CC} = Min	I_{OH} = 20 µA	V_{CC}−0.1		V
V_{OL}	Output LOW Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.5	V
		V_{CC} = Min	I_{OL} = 6 mA		0.33	V
			I_{OL} = 20 µA		0.1	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Notes 1, 2)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Notes 1, 2)			0.9	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			−10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max V_{IN} = V_{IH} or V_{IL} (Note 3)			−10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)		−5	−150	mA
I_{CC}	Supply Current	Outputs Open (I_{OUT} = 0 mA)	f = 0 MHz		30	µA
		V_{CC} = Max	f = 15 MHz		120	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2. Represents the worst case of HC and HCT standards, allowing compatibility with either.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Condition		Typ	Unit
C_IN	Input Capacitance	V_IN = 2.0 V	V_CC = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_OUT	Output Capacitance	V_OUT = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.
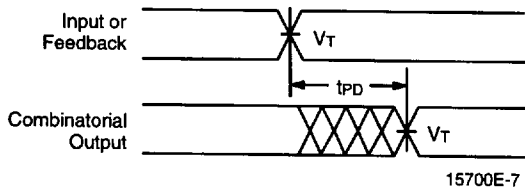
SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			Min	Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output (Note 3)				25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{AR}	Asynchronous Reset to Registered Output				25	ns
t_{ARW}	Asynchronous Reset Width			25		ns
t_{ARR}	Asynchronous Reset Recovery Time			25		ns
t_{SPR}	Synchronous Preset Recovery Time			25		ns
t_{WL}	Clock Width	LOW		10		ns
t_{WH}		HIGH		10		ns
f_{MAX}	Maximum Frequency (Notes 4 and 5)	External Feedback	$1/(t_S + t_{CO})$	33.3		MHz
		Internal Feedback (f_{CNT})	$1/(t_S + t_{CF})$	35.7		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	50		MHz
t_{EA}	Input to Output Enable Using Product Term Control				25	ns
t_{ER}	Input to Output Disable Using Product Term Control				25	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. This parameter is tested in Standby Mode. When the device is not in Standby Mode, the t_{PD} will typically be 5 ns faster.

4. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.

5. t_{CF} is a calculated value and is not guaranteed. t_{CF} can be found using the following equation:
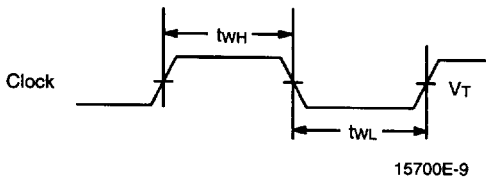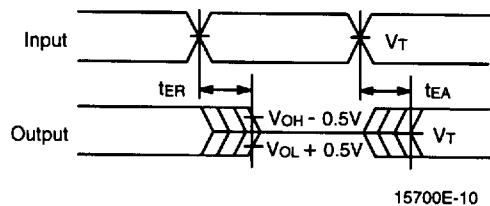$t_{CF} = 1/f_{MAX}$ (internal feedback) $- t_S$.
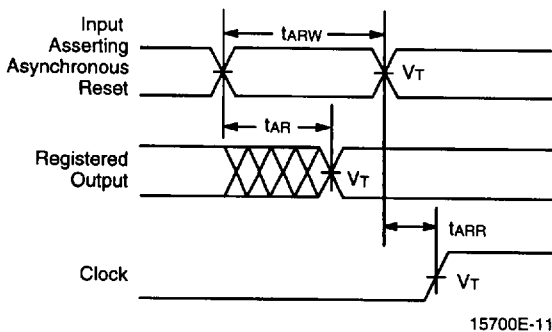
SWITCHING WAVEFORMS

Combinatorial Output
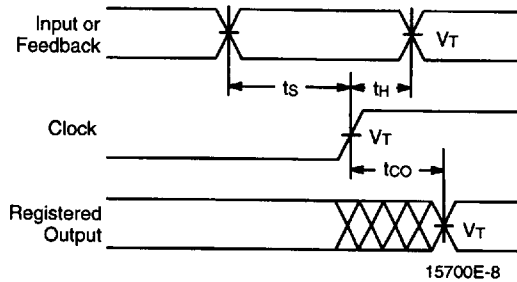
15700E-7

Registered Output

15700E-8

Clock Width

15700E-9

Input to Output Disable/Enable

15700E-10

Asynchronous Reset

15700E-11

Synchronous Preset

15700E-12
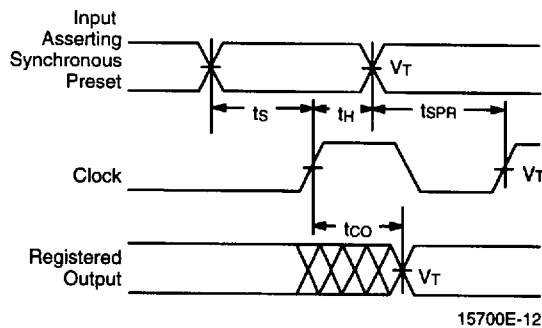
Notes:

1. $V_T = 1.5$ V for input signals and $V_{CC}/2$ for output signals.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 ns–5 ns typical.

KEY TO SWITCHING WAVEFORMS

| WAVEFORM	INPUTS	OUTPUTS
———	Must be Steady	Will be Steady
\\\\\	May Change from H to L	Will be Changing from H to L
/////	May Change from L to H	Will be Changing from L to H
XXXXX	Don't Care, Any Change Permitted	Changing, State Unknown
>—<	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING TEST CIRCUIT

Vcc
S1
R1
Output — Test Point
R2   CL
S2
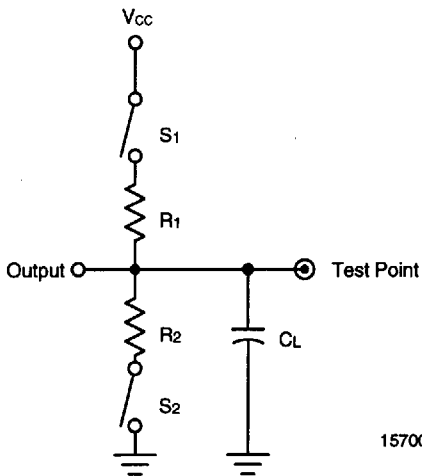
15700E-13

Specification	S₁	S₂	C_L	R₁	R₂	Measured Output Value
tₚD, tCO	Closed	Closed				Vcc/2
tEA	Z → H: Open Z → L: Closed	Z → H: Closed Z → L: Open	30 pF	820 Ω	820 Ω	Vcc/2
tER	H → Z: Open L → Z: Closed	H → Z: Closed L → Z: Open	5 pF			H → Z: V_OH − 0.5 V L → Z: V_OL + 0.5 V

TYPICAL Icc CHARACTERISTICS FOR THE PALCE22V10Z-15
Vcc = 5.0 V, TA = 25°C
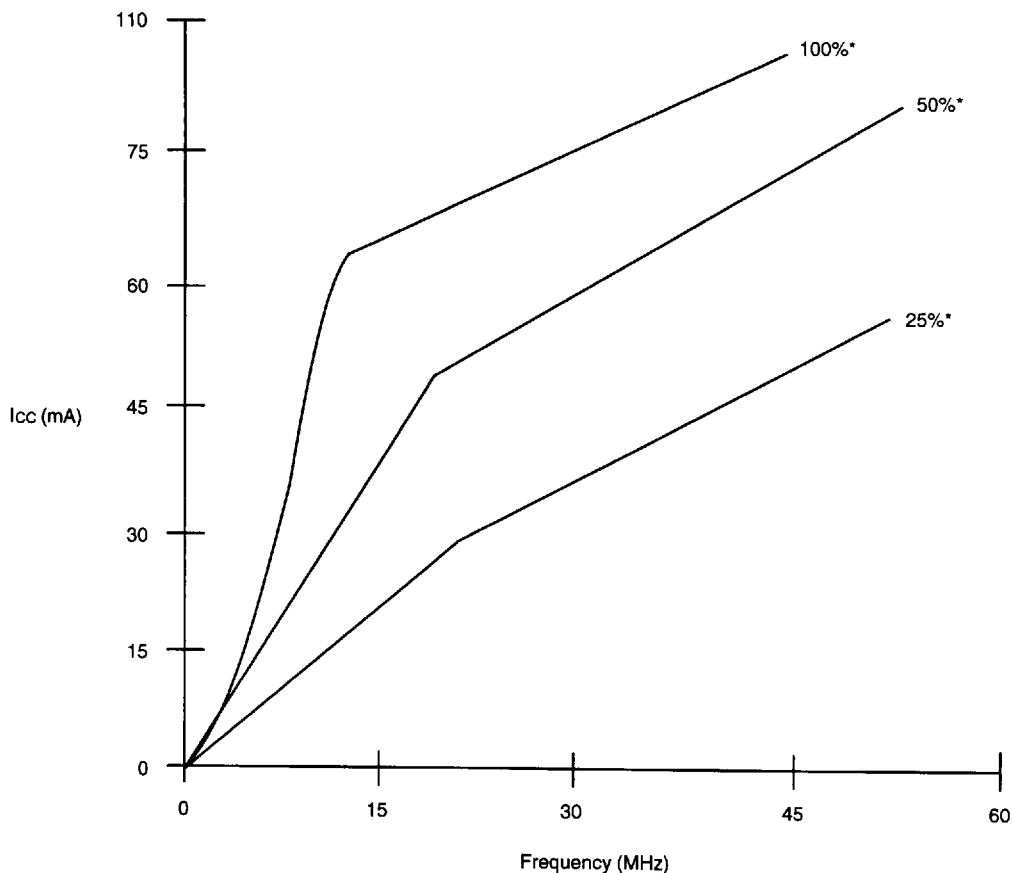
Percent of product terms used.
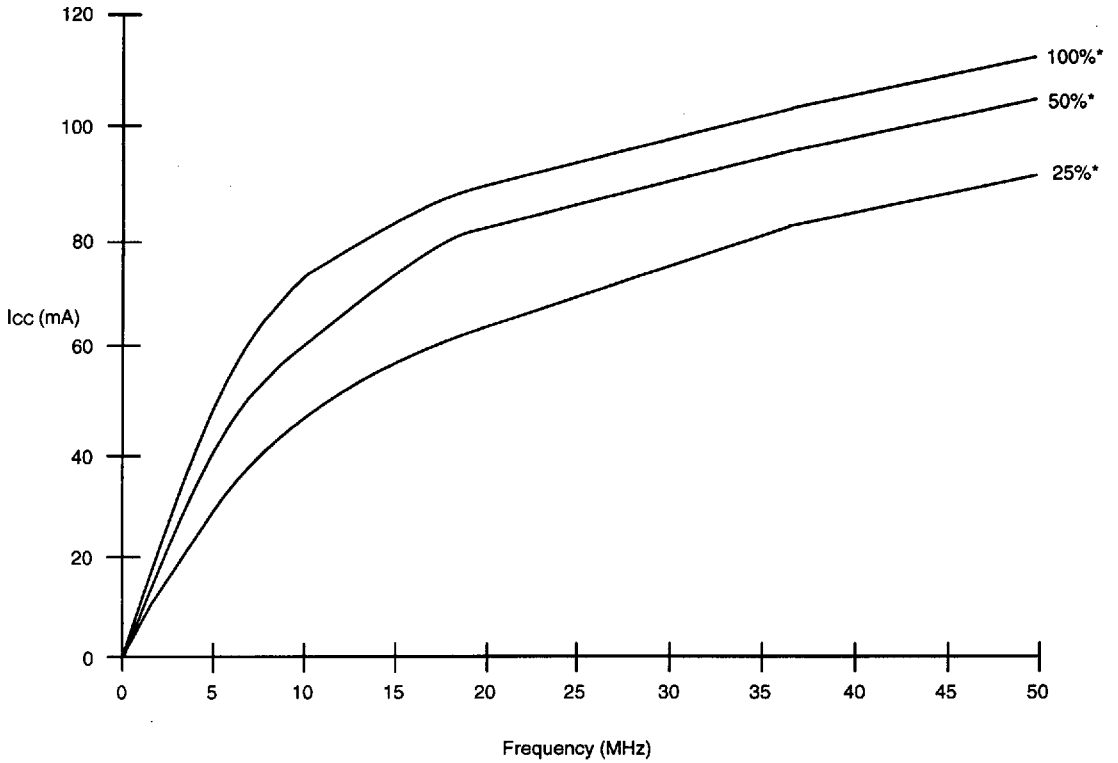
15700E-14

Icc vs. Frequency
Graph for the PALCE22V10Z-15

TYPICAL I_CC CHARACTERISTICS FOR THE PALCE22V10Z-25
$V_{CC} = 5.0\ V$, $T_A = 25°C$

*Percent of product terms used.

15700E-15

**I_CC vs. Frequency
Graph for the PALCE22V10Z-25**

0257526 0036863 2T9

ENDURANCE CHARACTERISTICS

The PALCE22V10Z is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

Endurance Characteristics

| Symbol	Parameter	Test Conditions	Min	Unit
tDR	Min Pattern Data Retention Time	Max Storage Temperature	10	Years
		Max Operating Temperature	20	Years
N	Min Reprogramming Cycles	Normal Programming Conditions	100	Cycles

ROBUSTNESS FEATURES

The PALCE22V10Z has some unique features that make it extremely robust, especially when operating in high speed design environments. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns.

INPUT/OUTPUT EQUIVALENT SCHEMATICS
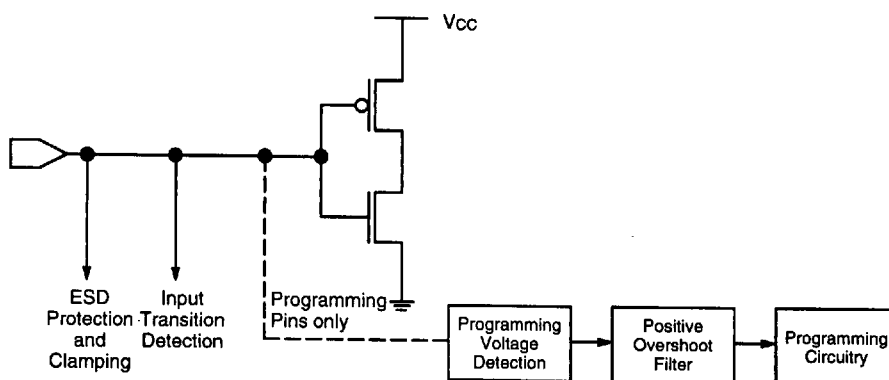
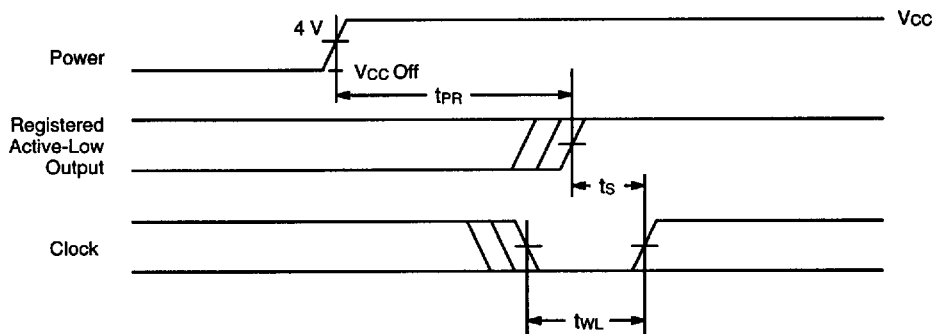**Typical Input**
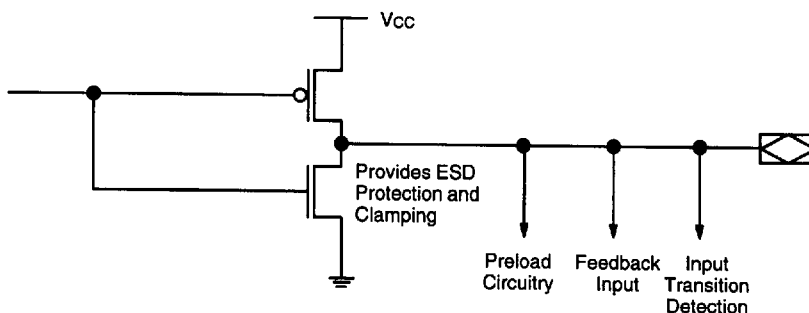
Typical Output

15700E-16

POWER-UP RESET FOR THE PALCE22V10Z FAMILY

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways Vcc can rise to its steady state, four conditions are required to ensure a valid power-up reset. These conditions are:

■ The supply voltage prior to the Vcc rise must not exceed Vcc off.

■ The Vcc rise must be monotonic.

■ Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

■ If inputs are not switching at the time of power-up, an input transition must take place to assure proper data is set-up in registers or to outputs.

Parameter Symbol	Parameter Description	Max	Unit
tPR	Power-Up Reset Time	1000	ns
ts	Input or Feedback Setup Time	See Switching Characteristics	
tWL	Clock Width LOW		
Vcc Off	Supply Voltage Prior to Power-Up	100	mV

Power-Up Reset Waveform

15700E-17