Theory and Applications of the MC34063 and μA78S40 Switching Regulator Control Circuits

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APPLICATION NOTE

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This paper describes in detail the principle of operation of the MC34063 and μA78S40 switching regulator subsystems. Several converter design examples and numerous applications circuits with test data are included.

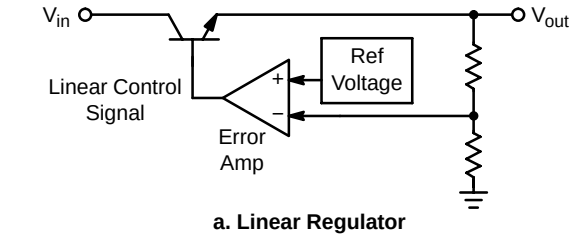
INTRODUCTION

The MC34063 and μA78S40 are monolithic switching regulator subsystems intended for use as dc to dc converters. These devices represent a significant advancement in the ease of implementing highly efficient and yet simple switching power supplies. The use of switching regulators is becoming more pronounced over that of linear regulators because the size reductions in new equipment designs require greater conversion efficiency. Another major advantage of the switching regulator is that it has increased application flexibility of output voltage. The output can be less than, greater than, or of opposite polarity to that of the input voltage.

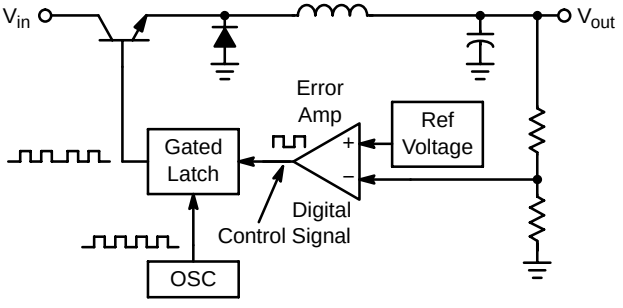
PRINCIPLE OF OPERATION

In order to understand the difference in operation between linear and switching regulators we must compare the block diagrams of the two step−down regulators shown in Figure 1. The linear regulator consists of a stable reference, a high gain error amplifier, and a variable resistance series−pass element. The error amplifier monitors the output voltage level, compares it to the reference and generates a linear control signal that varies between two extremes, saturation and cutoff. This signal is used to vary the resistance of the series−pass element in a corrective fashion in order to maintain a constant output voltage under varying input voltage and output load conditions.

The switching regulator consists of a stable reference and a high gain error amplifier identical to that of the linear regulator. This system differs in that a free running oscillator and a gated latch have been added. The error amplifier again monitors the output voltage, compares it to the reference level and generates a control signal. If the output voltage is below nominal, the control signal will go to a high state and turn on the gate, thus allowing the oscillator clock pulses to drive the series−pass element alternately from cutoff to saturation. This will continue until the output voltage is pumped up slightly above its nominal value. At this time, the control signal will go low and turn off the gate, terminating any further switching of the series−pass element. The output voltage will eventually decrease to below nominal due to the presence of an external load, and will initiate the switching process again. The increase in conversion efficiency is primarily due to the operation of the series−pass element only in the saturated or cutoff state. The voltage drop across the element, when saturated, is small as is the dissipation. When in cutoff, the current through the element and likewise the power dissipation are also small. There are other variations of switching control. The most common are the fixed frequency pulse width modulator and the fixed on−time variable off−time types, where the on−off switching is uninterrupted and regulation is achieved by duty cycle control. Generally speaking, the example given in Figure 1b does apply to MC34063 and μA78S40.



a. Linear Regulator



b. Switching Regulator

Figure 1. Step−Down Regulators

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GENERAL DESCRIPTION

The MC34063 series is a monolithic control circuit containing all the active functions required for dc to dc converters. This device contains an internal temperature compensated reference, comparator, controlled duty cycle oscillator with an active peak current limit circuit, driver, and a high current output switch. This series was specifically designed to be incorporated in step−up, step−down and voltage−inverting converter applications. These functions are contained in an 8−pin dual in−line package shown in Figure 2a.

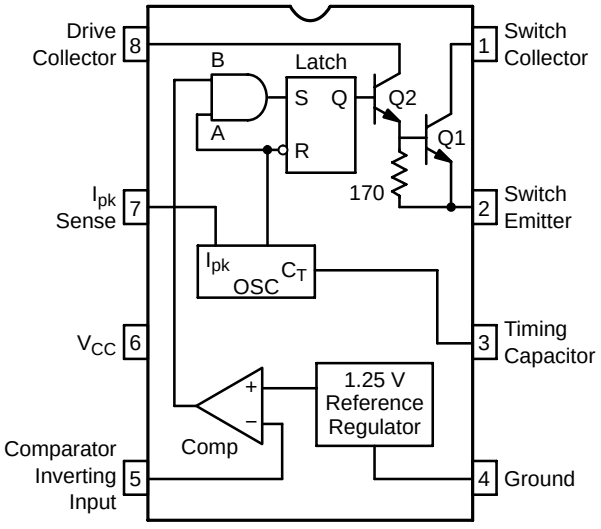
The μA78S40 is identical to the MC34063 with the addition of an on−board power catch diode, and an uncommitted operational amplifier. This device is in a 16−pin dual in−line package which allows the reference and the noninverting input of the comparator to be pinned out. These additional features greatly enhance the flexibility of this part and allow the implementation of more sophisticated applications. These may include series−pass regulation of the main output or of a derived second output voltage, a tracking regulator configuration or even a second switching regulator.

FUNCTIONAL DESCRIPTION

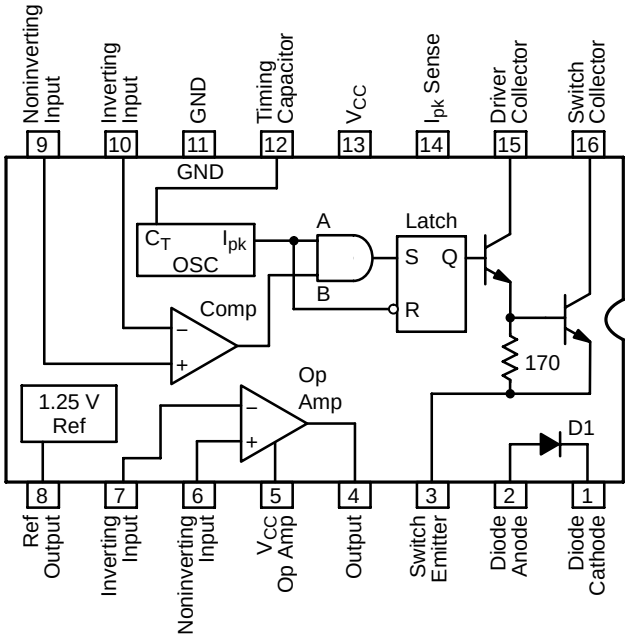
The oscillator is composed of a current source and sink which charges and discharges the external timing capacitor C_T between an upper and lower preset threshold. The typical charge and discharge currents are 35 μA and 200 μA respectively, yielding about a one to six ratio. Thus the ramp−up period is six times longer than that of the ramp−down as shown in Figure 3. The upper threshold is equal to the internal reference voltage of 1.25 V and the lower is approximately equal to 0.75 V. The oscillator runs continuously at a rate controlled by the selected value of C_T.

During the ramp−up portion of the cycle, a Logic “1” is present at the “A” input of the AND gate. If the output voltage of the switching regulator is below nominal, a Logic “1” will also be present at the “B” input. This condition will set the latch and cause the “Q” output to go to a Logic “1”, enabling the driver and output switch to conduct. When the oscillator reaches its upper threshold, C_T will start to discharge and Logic “0” will be present at the “A” input of the AND gate. This logic level is also connected to an inverter whose output presents a Logic “1” to the reset input of the latch. This condition will cause “Q” to go low, disabling the driver and output switch. A logic truth table of these functional blocks is shown in Figure 4.

The output of the comparator can set the latch only during the ramp−up of C_T and can initiate a partial or full on−cycle of output switch conduction. Once the comparator has set the latch, it cannot reset it. The latch will remain set until C_T begins ramping down. Thus the comparator can initiate output switch conduction, but cannot terminate it and the latch is always reset when C_T begins ramping down. The comparator’s output will be at a Logic “0” when the output voltage of the switching regulator is above nominal. Under these conditions, the comparator’s output can inhibit a portion of the output switch on−cycle, a complete cycle, a complete cycle plus a portion of one cycle, multiple cycles, or multiple cycles plus a portion of one cycle.



a. MC34063



b. μA78S40

Figure 2. Functional Block Diagrams

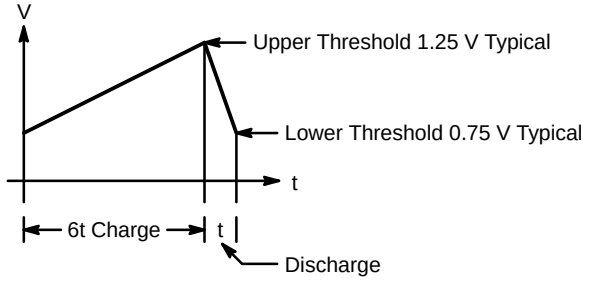


Figure 3. C_T Voltage Waveform

Active Condition of Timing Capacitor, C_T	AND Gate Inputs		Latch Inputs		Output Switch	Comments on State of Output Switch
	A	B	S	R		
Begins Ramp−Up		0	0		0	Switching regulator's output is ≥ nominal ('B' = 0).
Begins Ramp−Down		0	0		0	No change since 'B' was 0 before C_T Ramp−Down.
Ramping Down	0		0	1	0	No change even though switching regulator's output < nominal. Output switch cannot be initiated during R_T Ramp−Down.
Ramping Down	0		0	1	0	No change since output switch conduction was terminated when 'A' went to 0.
Ramping Up	1			0		Switching regulator's output went < nominal during C_T Ramp−Up ('B' → 1). Partial on−cycle for output switch.
Ramping Up	1			0	1	Switching regulator's output went ≥ nominal ('B' → 0) during C_T Ramp−Up. No change since 'B' cannot reset latch.
Begins Ramp−Up		1				Complete on−cycle since 'B' was 1 before C_T started Ramp−Up.
Begins Ramp−Down		1				Output switch conduction is always terminated whenever C_T is Ramping Down.

Figure 4. Logic Truth Table of Functional Blocks

Current limiting is accomplished by monitoring the voltage drop across an external sense resistor placed in series with V_{CC} and the output switch. The voltage drop developed across this resistor is monitored by the I_{pk} Sense pin. When this voltage becomes greater than 330 mV, the current limit circuitry provides an additional current path to charge the timing capacitor C_T. This causes it to rapidly reach the upper oscillator threshold, thereby shortening the time of output switch conduction and thus reducing the amount of energy stored in the inductor. This can be observed as an increase in the slope of the charging portion of the C_T voltage waveform as shown in Figure 5. Operation of the switching regulator in an overload or shorted condition will cause a very short but finite time of output conduction followed by either a normal or extended off−time internal provided by the oscillator ramp−down time of C_T. The extended interval is the result of charging C_T beyond the upper oscillator threshold by overdriving the current limit sense input. This can be caused by operating the switching regulator with a severely overloaded or shorted output or having the input voltage grossly above the nominal design value.

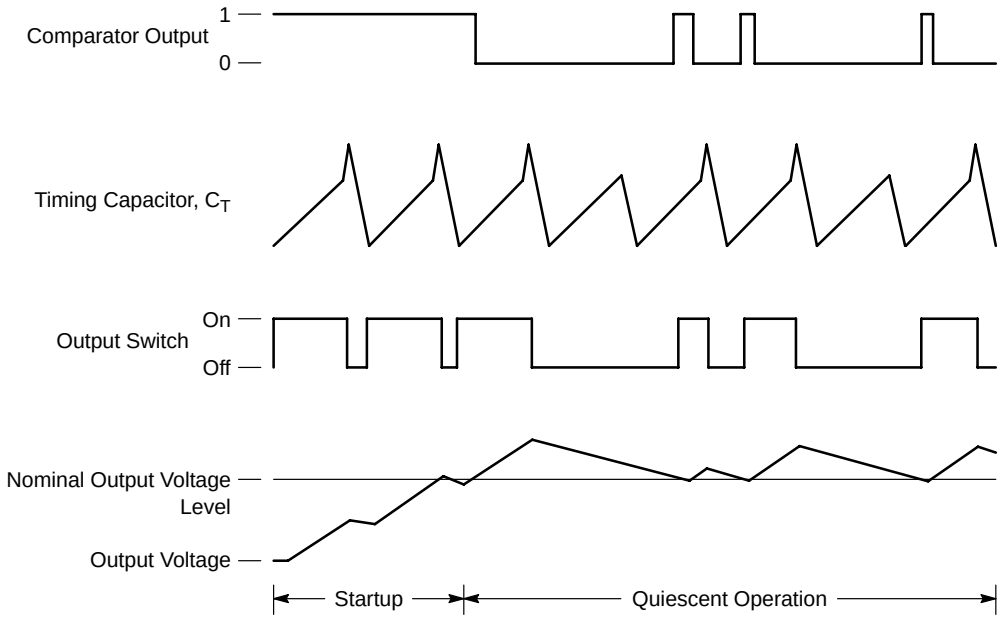


Figure 5. Typical Operating Waveforms

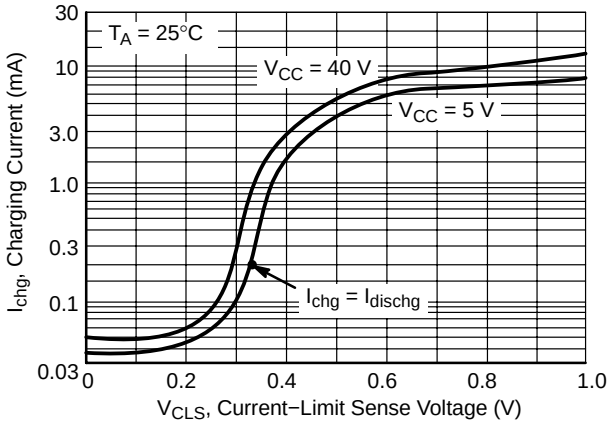


Figure 6. Timing Capacitor Charge Current versus Current−Limit Sense Voltage

Under extreme conditions, the voltage across C_T will approach V_{CC} and can cause a relatively long off−time. This action may be considered a feature since it will reduce the power dissipation of the output switch considerably. This feature may be disabled on the µA78S40 only, by connecting a small signal PNP transistor as a clamp. The emitter is connected to C_T, the base to the reference output, and the collector to ground. This will limit the maximum charge voltage across C_T to less than 2.0 V. With the use of current limiting, saturation of the storage inductor may be prevented as well as achieving a soft startup.

In practice the current limit circuit will somewhat modify the charging slope and peak amplitude of C_T each time the output switch is required to conduct. This is because the threshold voltage of the current limit sense circuit exhibits a “soft” voltage turn−on characteristic and has a turn−off time delay that causes some overshoot. The 330 mV threshold is defined where the charge and discharge currents are of equal value with V_{CC} = 5.0 V, as shown in Figure 6. The current limit sense circuit can be disabled by connecting the I_{pk} Sense pin to V_{CC}.

To aid in system design flexibility, the driver collector, output switch collector and emitter are pinned out separately. This allows the designer the option of driving the output switch transistor into saturation with a selected forced gain or driving it near saturation when connected as a Darlington. The output switch has a typical current gain of 70 at 1.0 A and is designed to switch a maximum of 40 V collector−to−emitter, with up to 1.5 A peak collector current.

The µA78S40 has the additional features of an on−chip uncommitted operational amplifier and catch diode. The op amp is a high gain single supply type with an input common−mode voltage range that includes ground. The output is capable of sourcing up to 150 mA and sinking 35 mA. A separate V_{CC} pin is provided in order to reduce the integrated circuit standby current and is useful in low power applications if the operational amplifier is not incorporated into the main switching system. The catch diode is constructed from a lateral PNP transistor and is capable of blocking up to 40 V and will conduct current up to 1.5 A. There is, however, a “catch” when using it.

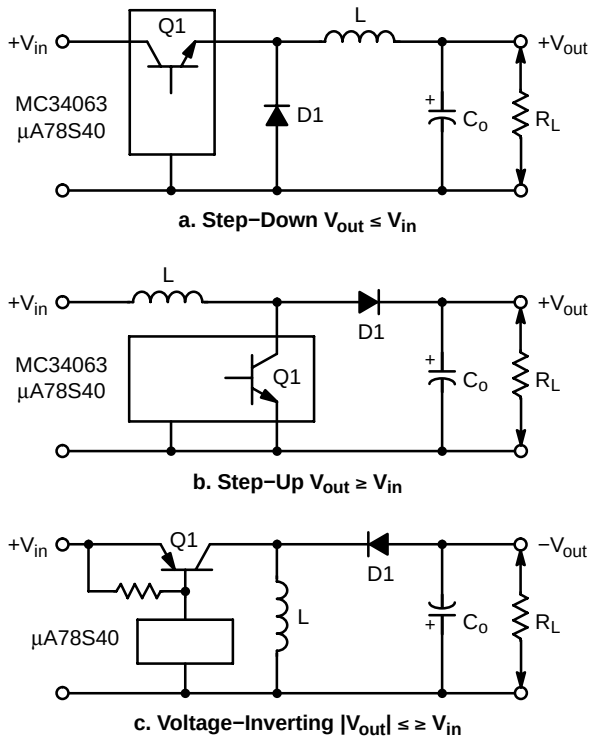


Figure 7. Basic Switching Regulator Configurations

Because the integrated circuit substrate is common with the internal and external circuitry ground, the cathode of the diode cannot be operated much below ground or forward biasing of the substrate will result. This totally eliminates the diode from being used in the basic voltage inverting configuration as in Figure 15, since the substrate, pin 11, is common to ground. The diode can be considered for use only in low power converter applications where the total system component count must be held to a minimum. The substrate current will be about 10 percent of the catch diode current in the step−up configuration and about 20 percent in the step−down and voltage−inverting in which pin 11 is common to the negative output. System efficiency will suffer when using this diode and the package dissipation limits must be observed.

STEP−DOWN SWITCHING REGULATOR OPERATION

Shown in Figure 7a is the basic step−down switching regulator. Transistor Q1 interrupts the input voltage and provides a variable duty cycle squarewave to a simple LC filter. The filter averages the squarewaves producing a dc output voltage that can be set to any level less than the input by controlling the percent conduction time of Q1 to that of the total switching cycle time. Thus,

$$V_{out} = V_{in}(\%\ t_{on}) \text{ or } V_{out} = V_{in}\left(\frac{t_{on}}{t_{on} + t_{off}}\right)$$

The MC34063/µA78S40 achieves regulation by varying the on−time and the total switching cycle time. An explanation of the step−down converter operation is as follows: Assume that the transistor Q1 is off, the inductor current I_L is zero, and the output voltage V_{out} is at its nominal

value. The output voltage across capacitor C_o will eventually decay below nominal because it is the only component supply current into the external load R_L. This voltage deficiency is monitored by the switching control circuit and causes it to drive Q1 into saturation. The inductor current will start to flow from V_{in} through Q1 and, C_o in parallel with R_L, and rise at a rate of $\Delta I/\Delta T = V/L$. The voltage across the inductor is equal to $V_{in} - V_{sat} - V_{out}$ and the peak current at any instant is:

$$I_L = \left(\frac{V_{in} - V_{sat} - V_{out}}{L}\right) t$$

At the end of the on−time, Q1 is turned off. As the magnetic field in the inductor starts to collapse, it generates a reverse voltage that forward biases D1, and the peak current will decay at a rate of $\Delta I/\Delta T = V/L$ as energy is supplied to C_o and R_L. The voltage across the inductor during this period is equal to $V_{out} + V_F$ of D1, and the current at any instant is:

$$I_L = I_{L(pk)} - \left(\frac{V_{out} + V_F}{L}\right) t$$

Assume that during quiescent operation the average output voltage is constant and that the system is operating in the discontinuous mode. Then $I_{L(peak)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be determined.

$$\left(\frac{V_{in} - V_{sat} - V_{out}}{L}\right) t_{on} = \left(\frac{V_{out} + V_F}{L}\right) t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F}{V_{in} - V_{sat} - V_{out}}$$

Note that the volt−time product of t_{on} must be equal to that of t_{off} and the inductance value is not of concern when determining their ratio. If the output voltage is to remain constant, the average current into the inductor must be equal to the output current for a complete cycle. The peak inductor current with respect to output current is:

$$\left(\frac{I_{L(pk)}}{2}\right) t_{on} + \left(\frac{I_{L(pk)}}{2}\right) t_{off} = (I_{out}\, t_{on}) + (I_{out}\, t_{off})$$

$$\frac{I_{L(pk)}(t_{on} + t_{off})}{2} = I_{out}\,(t_{on} + t_{off})$$

$$\therefore I_{L(pk)} = 2\, I_{out}$$

The peak inductor current is also equal to the peak switch current $I_{pk(switch)}$ since the two are in series. The on−time, t_{on}, is the maximum possible switch conduction time. It is equal to the time required for C_T to ramp up from its lower to upper threshold. The required value for C_T can be determined by using the minimum oscillator charging current and the typical value for the oscillator voltage swing both taken from the data sheet electrical characteristics table.

$$C_T = I_{chg(min)} \left(\frac{\Delta t}{\Delta V}\right)$$

$$= 20 \times 10^{-6} \left(\frac{t_{on}}{0.5}\right)$$

$$= 4.0 \times 10^{-5}\, t_{on}$$

The off−time, t_{off}, is the time that diode D1 is in conduction and it is determined by the time required for the inductor current to return to zero. The off−time is not related to the ramp−down time of C_T. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$ and the minimum operating frequency is:

$$f_{min} = \frac{1}{t_{on(max)} + t_{off}}$$

A minimum value of inductance can now be calculated for L. The known quantities are the voltage across the inductor and the required peak current for the selected switch conduction time.

$$L_{min} = \frac{V_{in} - V_{sat} - V_{out}}{I_{pk(switch)}}\, t_{on}$$

This minimum value of inductance was calculated by assuming the onset of continuous conduction operation with a fixed input voltage, maximum output current, and a minimum charge−current oscillator.

The net charge per cycle delivered to the output filter capacitor C_o, must be zero, $Q+ = Q-$, if the output voltage is to remain constant. The ripple voltage can be calculated from the known values of on−time, off−time, peak inductor current, and output capacitor value.

$$V_{ripple(p-p)} = \left(\frac{1}{C_o}\right) \int_0^{t_1} i\,t\,dt + \left(\frac{1}{C_o}\right) \int_{t_1}^{t_2} i'\,t\,dt$$

where $i\,t = \frac{\frac{1}{2} I_{pk} t}{t_{on}/2}$ and $i'\,t = \frac{\frac{1}{2} I_{pk} t}{t_{off}/2}$

$$= \frac{1}{C_o} \left| \frac{I_{pk}}{t_{on}} \frac{t^2}{2} \right|_0^{t_1} + \frac{1}{C_o} \left| \frac{I_{pk}}{t_{off}} \frac{t^2}{2} \right|_{t_1}^{t_2}$$

And $t_1 = \frac{t_{on}}{2}$ and $t_2 - t_1 = \frac{t_{off}}{2}$

Substituting for t_1 and $t_2 - t_1$ yields:

$$= \frac{1}{C_o} \frac{I_{pk}}{t_{on}} \frac{(t_{on}/2)^2}{2} + \frac{1}{C_o} \frac{I_{pk}}{t_{off}} \frac{(t_{off}/2)^2}{2}$$

$$= \frac{I_{pk}\,(t_{on} + t_{off})}{8\, C_o}$$

A graphical derivation of the peak−to−peak ripple voltage can be obtained from the capacitor current and voltage waveforms in Figure 8.

The calculations shown account for the ripple voltage contributed by the ripple current into an ideal capacitor. In practice, the calculated value will need to be increased due to the internal equivalent series resistance ESR of the capacitor. The additional ripple voltage will be equal to I_{pk}(ESR). Increasing the value of the filter capacitor will reduce the output ripple voltage. However, a point of diminishing return will be reached because the comparator requires a finite voltage difference across its inputs to control the latch. This voltage difference to completely change the latch states is about 1.5 mV and the minimum achievable ripple at the output will be the feedback divider ratio multiplied by 1.5 mV or:

$$V_{ripple(p-p)min} = \frac{V_{out}}{V_{ref}}\,(1.5 \times 10^{-3})$$

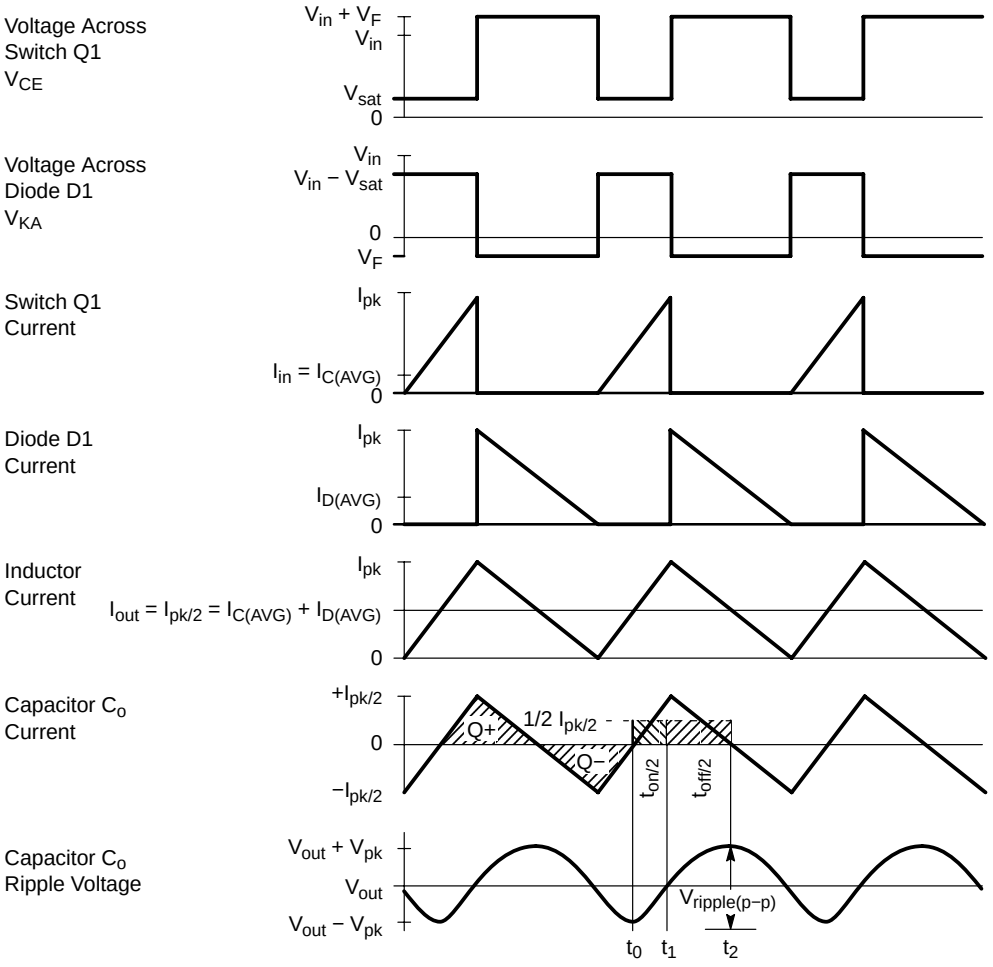


Figure 8. Step−Down Switching Regulator Waveforms

This problem becomes more apparent in a step−up converter with a high output voltage. Figures 12 and 13 show two different ripple reduction techniques. The first uses the μA78S40 operational amplifier to drive the comparator in the feedback loop. The second technique uses a Zener diode to level shift the output down to the reference voltage.

Step−Down Switching Regulator Design Example

A schematic of the basic step−down regulator is shown in Figure 9. The μA78S40 was chosen in order to implement a minimum component system, however, the MC34063 with an external catch diode can also be used. The frequency chosen is a compromise between switching losses and inductor size. There will be a further discussion of this and other design considerations later. Given are the following:

V_{out} = 5.0 V
I_{out} = 50 mA
f_{min} = 50 kHz
$V_{in(min)}$ = 24 V − 10% or 21.6 V
$V_{ripple(p-p)}$ = 0.5% V_{out} or 25 mV_{p-p}

1. Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$$

$$= \frac{5.0 + 0.8}{21.6 - 0.8 - 5.0}$$

$$= 0.37$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20\ \mu s \text{ per cycle}$$

3. Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2. By using substitution and some algebraic gymnastics, an equation can be written for t_{off} in terms of t_{on}/t_{off} and $t_{on} + t_{off}$.

The equation is:

$$t_{off} = \frac{t_{on(max)} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$

$$= \frac{20 \times 10^{-6}}{0.37 + 1}$$

$$= 14.6\ \mu s$$

Since $t_{on(max)} + t_{off} = 20\ \mu s$

$$t_{on(max)} = 20\ \mu s - 14.6\ \mu s$$

$$= 5.4\ \mu s$$

Note that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 6/7 or 0.857. This maximum is defined by the 6:1 ratio of charge−to−discharge current of timing capacitor C_T (refer to Figure 3).

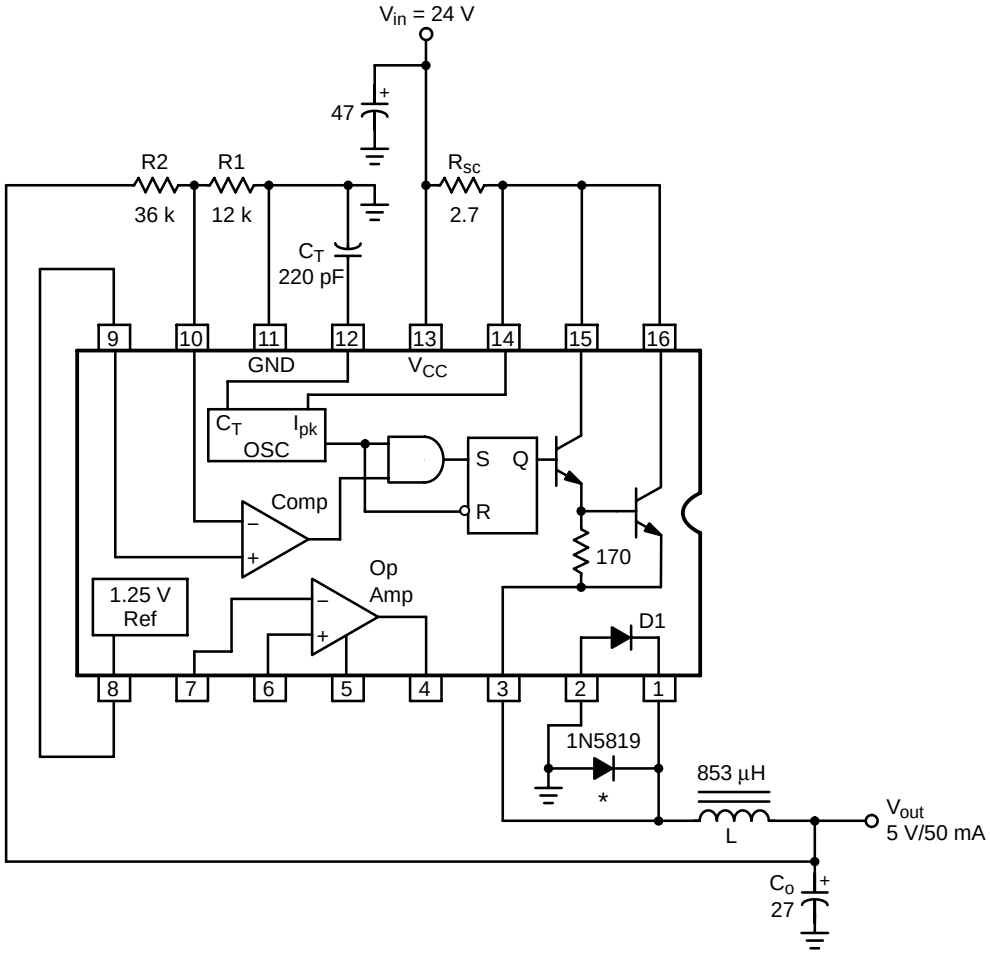
4. The maximum on−time, $t_{on(max)}$, is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5}\ t_{on}$$

$$= 4.0 \times 10^{-5}\ (5.4 \times 10^{-6})$$

$$= 216\ pF$$

Use a standard 220 pF capacitor.



Test	Conditions	Results
Line Regulation	V_{in} = 18 to 30 V, I_{out} = 50 mA	Δ = 16 mV or ± 0.16%
Load Regulation	V_{in} = 24 V, I_{out} = 25 to 50 mA	Δ = 28 mV or ± 0.28%
Output Ripple	V_{in} = 21.6 V, I_{out} = 50 mA	24 mV_{p-p}
Short Circuit Current	V_{in} = 24 V, R_L = 0.1 Ω	105 mA
Efficiency, Internal Diode	V_{in} = 24 V, I_{out} = 50 mA	45.3%
Efficiency, External Diode*	V_{in} = 24 V, I_{out} = 50 mA	72.6%

Figure 9. Step−Down Design Example

5. The peak switch current is:

$$I_{pk(switch)} = 2\ I_{out}$$
$$= 2\ (50 \times 10^{-3})$$
$$= 100\ mA$$

6. With knowledge of the peak switch current and maximum on time, a minimum value of inductance can be calculated.

$$L_{min} = \left(\frac{V_{in(min)} - V_{sat} - V_{out}}{I_{pk(switch)}}\right) t_{on(max)}$$
$$= \left(\frac{21.6 - 0.8 - 5.0}{100 \times 10^{-3}}\right) 5.4 \times 10^{-6}$$
$$= 853\ \mu H$$

7. A value for the current limit resistor, R_{sc}, can be determined by using the current level of $I_{pk(switch)}$ when V_{in} = 24 V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat} - V_{out}}{L_{min}}\right) t_{on(max)}$$
$$= \left(\frac{24 - 0.8 - 5.0}{853 \times 10^{-6}}\right) 5.4 \times 10^{-6}$$
$$= 115\ mA$$
$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$
$$= \frac{0.33}{115 \times 10^{-3}}$$
$$= 2.86\ \Omega,\ \text{use } 2.7\ \Omega$$

This value may have to be adjusted downward to compensate for conversion losses and any increase in $I_{pk(switch)}$) current if V_{in} varies upward. Do not set R_{sc} to exceed the maximum $I_{pk(switch)}$ limit of 1.5 A when using the internal switch transistor.

8. A minimum value for an ideal output filter capacitor can now be obtained.

$$C_o = \frac{I_{pk(switch)}\ (t_{on} + t_{off})}{8\ V_{ripple(p-p)}}$$
$$= \frac{0.1\ (20 \times 10^{-6})}{8\ (25 \times 10^{-3})}$$
$$= 10\ \mu F$$

Ideally this would satisfy the design goal, however, even a solid tantalum capacitor of this value will have a typical ESR (equivalent series resistance) of 0.3 Ω which will contribute 30 mV of ripple. The ripple components are not in phase, but can be assumed to be for a conservative design. In satisfying the example shown, a 27 μF tantalum with an ESR of 0.1 Ω was selected. The ripple voltage should be kept to a low value since it will directly affect the system line and load regulation.

9. The nominal output voltage is programmed by the R1, R2 resistor divider. The output voltage is:

$$V_{out} = 1.25\left(\frac{R2}{R1} + 1\right)$$

The divider current can go as low as 100 μA without affecting system performance. In selecting a minimum current divider R1 is equal to:

$$R1 = \frac{1.25}{100 \times 10^{-6}}$$
$$= 12,500\ \Omega$$

Rearranging the above equation so that R2 can be solved yields:

$$R2 = R1\left(\frac{V_{out}}{1.25} - 1\right)$$

If a standard 5% tolerance 12 k resistor is chosen for R1, R2 will also be a standard value.

$$R2 = 12 \times 10^3\left(\frac{5.0}{1.25} - 1\right)$$
$$= 36\ k$$

Using the above derivation, the design is optimized to meet the assumed conditions. At $V_{in(min)}$, operation is at the onset of continuous mode and the output current capability will be greater than 50 mA. At $V_{in(nom)}$ i.e., 24 V, the current limit will activate slightly above the rated I_{out} of 50 mA.

STEP−UP SWITCHING REGULATOR OPERATION

The basic step−up switching regulator is shown in Figure 7b and the waveform is in Figure 10. Energy is stored in the inductor during the time that transistor Q1 is in the “on” state. Upon turn−off, the energy is transferred in series with V_{in} to the output filter capacitor and load. This configuration allows the output voltage to be set to any value greater than that of the input by the following relationship:

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right) + V_{in}\ \text{ or }\ V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

An explanation of the step−up converter’s operation is as follows. Initially, assume that transistor Q1 is off, the inductor current is zero, and the output voltage is at its nominal value. At this time, load current is being supplied only by C_o and it will eventually fall below nominal. This deficiency will be sensed by the control circuit and it will initiate an on−cycle, driving Q1 into saturation. Current will start to flow from V_{in} through the inductor and Q1 and rise at a rate of ΔI/ΔT = V/L. The voltage across the inductor is equal to V_{in} − V_{sat} and the peak current is:

$$I_L = \left(\frac{V_{in} - V_{sat}}{L}\right) t$$

When the on−time is completed, Q1 will turn off and the magnetic field in the inductor will start to collapse generating a reverse voltage that forward biases D1, supplying energy to C_o and R_L. The inductor current will decay at a rate of ΔI/ΔT = V/L and the voltage across it is equal to V_{out} + V_F − V_{in}. The current at any instant is:

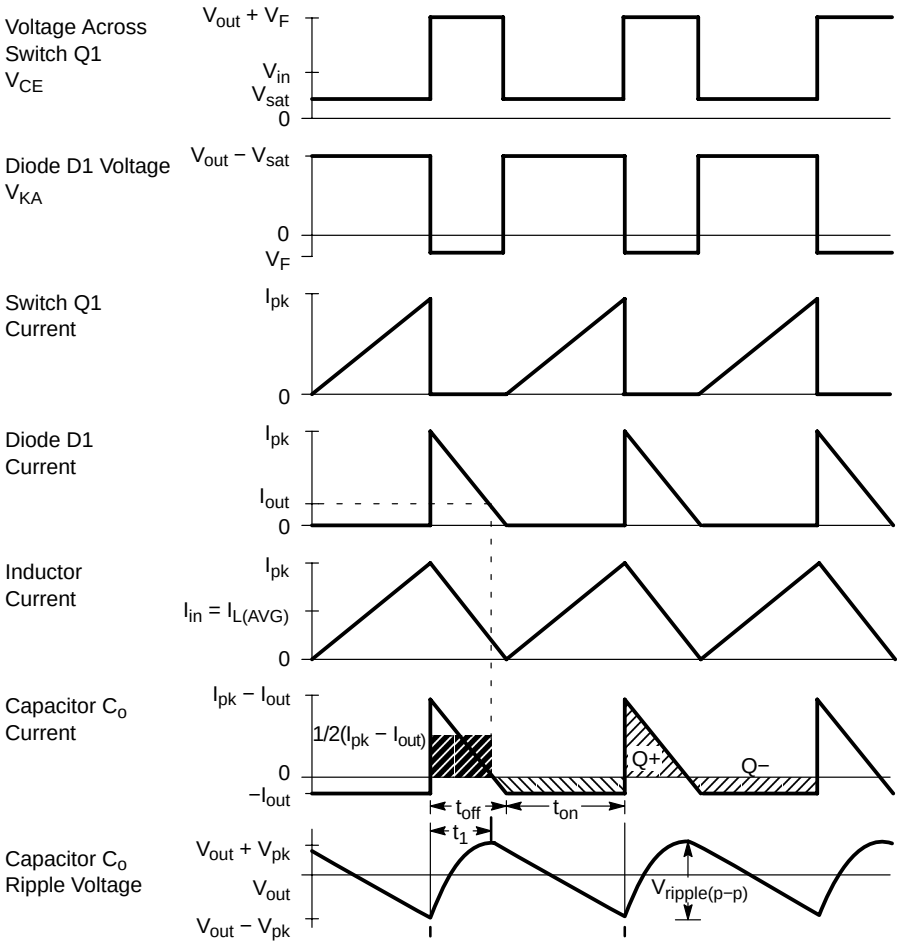


Figure 10. Step−Up Switching Regulator Waveforms

$$I_L = I_{L(pk)} - \left(\frac{V_{out} + V_F - V_{in}}{L}\right) t$$

Assuming that the system is operating in the discontinuous mode, the current through the inductor will reach zero after the t_{off} period is completed. Then $I_{L(pk)}$ attained during t_{on} must decay to zero during t_{off} and a ratio of t_{on} to t_{off} can be written.

$$\left(\frac{V_{in} - V_{sat}}{L}\right) t_{on} = \left(\frac{V_{out} + V_F - V_{in}}{L}\right) t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F - V_{in}}{V_{in} - V_{sat}}$$

Note again, that the volt−time product of t_{on} must be equal to that of t_{off} and the inductance value does not affect this relationship.

The inductor current charges the output filter capacitor through diode D1 only during t_{off}. If the output voltage is to remain constant, the net charge per cycle delivered to the output filter capacitor must be zero, Q+ = Q−.

$$I_{chg}\, t_{off} = I_{dischg}\, t_{on}$$

Figure 10 shows the step−up switching regulator waveforms. By observing the capacitor current and making some substitutions in the above statement, a formula for peak inductor current can be obtained.

$$\left(\frac{I_{L(pk)}}{2}\right) t_{off} = I_{out}\,(t_{on} + t_{off})$$

$$I_{L(pk)} = 2\, I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$

The peak inductor current is also equal to the peak switch current, since the two are in series.

With knowledge of the voltage across the inductor during t_{on} and the required peak current for the selected switch conduction time, a minimum inductance value can be determined.

$$L_{min} = \left(\frac{V_{in} - V_{sat}}{I_{pk(switch)}}\right) t_{on(max)}$$

The ripple voltage can be calculated from the known values of on−time, off−time, peak inductor current, output current and output capacitor value. Referring to the

capacitor current waveforms in Figure 10, t_1 is defined as the capacitor charging interval. Solving for t_1 in known terms yields:

$$\frac{I_{pk} - I_{out}}{t_1} = \frac{I_{pk}}{t_{off}}$$

$$\therefore t_1 = \left(\frac{I_{pk} - I_{out}}{I_{pk}}\right) t_{off}$$

And the current during t_1 can be written:

$$I = \left(\frac{I_{pk} - I_{out}}{t_1}\right) t$$

The ripple voltage is:

$$V_{ripple(p-p)} = \left(\frac{1}{C_o}\right) \int_0^{t_1} \frac{I_{pk} - I_{out}}{t_1} \, t \, dt$$

$$= \frac{1}{C_o} \left| \frac{I_{pk} - I_{out}}{t_1} \frac{t^2}{2} \right|_0^{t_1}$$

$$= \frac{1}{C_o} \frac{(I_{pk} - I_{out})}{2} t_1$$

Substituting for t_1 yields:

$$= \frac{1}{C_o} \frac{(I_{pk} - I_{out})}{2} \frac{(I_{pk} - I_{out})}{I_{pk}} t_{off}$$

$$= \frac{(I_{pk} - I_{out})^2 \, t_{off}}{2 \, I_{pk} \, C_o}$$

A simplified formula that will give an error of less than 5% for a voltage step−up greater than 3 with an ideal capacitor is shown:

$$V_{ripple(p-p)} \approx \left(\frac{I_{out}}{C_o}\right) t_{on}$$

This neglects a small portion of the total Q− area. The area neglected is equal to:

$$A = (t_{off} - t_1) \frac{I_{out}}{2}$$

Step−Up Switching Regulator Design Example

The basic step−up regulator schematic is shown in Figure 11. The μA78S40 again was chosen in order to implement a minimum component system. The following conditions are given:

V_{out} = 28 V
I_{out} = 50 mA
f_{min} = 50 kHz
$V_{in(min)}$ = 9.0 V − 25% or 6.75 V
$V_{ripple(p-p)}$ = 0.5% V_{out} or 140 mV_{p-p}

1. Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$$

$$= \frac{28 + 0.8 - 6.75}{6.75 - 0.3}$$

$$= 3.42$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20 \text{ μs per cycle}$$

3. Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2.

$$t_{off} = \frac{20 \times 10^{-6}}{3.42 + 1}$$

$$= 4.5 \text{ μs}$$

$$t_{on} = 20 \text{ μs} - 4.5 \text{ μs}$$

$$= 15.5 \text{ μs}$$

Note that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 0.857.

4. The maximum on−time, $t_{on(max)}$, is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5} \, t_{on}$$

$$= 4.0 \times 10^{-5} \, (15.5 \times 10^{-6})$$

$$= 620 \text{ pF}$$

5. The peak switch current is:

$$I_{pk(switch)} = 2 \, I_{out} \left(\frac{t_{on}}{t_{off}} + 1\right)$$

$$= 2 \, (50 \times 10^{-3}) \, (3.42 + 1)$$

$$= 442 \text{ mA}$$

6. A minimum value of inductance can be calculated since the maximum on−time and peak switch current are known.

$$L_{min} = \left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on}$$

$$= \left(\frac{6.75 - 0.3}{442 \times 10^{-3}}\right) 15.5 \times 10^{-6}$$

$$= 226 \text{ μH}$$

7. A value for the current limit resistor, R_{sc}, can now be determined by using the current level of $I_{pk(switch)}$ when V_{in} = 9.0 V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat}}{L_{min}}\right) t_{on(max)}$$

$$= \left(\frac{9.0 - 0.3}{226 \times 10^{-6}}\right) 15.5 \times 10^{-6}$$

$$= 597 \text{ mA}$$

$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{597 \times 10^{-3}}$$

$$= 0.55\ \Omega, \text{ use } 0.5\ \Omega$$

Note that current limiting in this basic step−up configuration will only protect the switch transistor from overcurrent due to inductor saturation. If the output is severely overloaded or shorted, D1, L, or R_{sc} may be destroyed since they form a direct path from V_{in} to V_{out}. Protection may be achieved by current limiting V_{in} or replacing the inductor with 1:1 turns ratio transformer.

8. An approximate value for an ideal output filter capacitor is:

$$C_o \approx \frac{I_{out}}{V_{ripple(p-p)}} t_{on}$$

$$\approx \frac{50 \times 10^{-3}}{140 \times 10^{-3}} 15.5 \times 10^{-6}$$

$$\approx 5.5\ \mu\text{F}$$

The ripple contribution due to the gain of the comparator:

$$V_{ripple(p-p)} = \frac{V_{out}}{V_{ref}} 1.5 \times 10^{-3}$$

$$= \frac{28}{1.25} 1.5 \times 10^{-3}$$

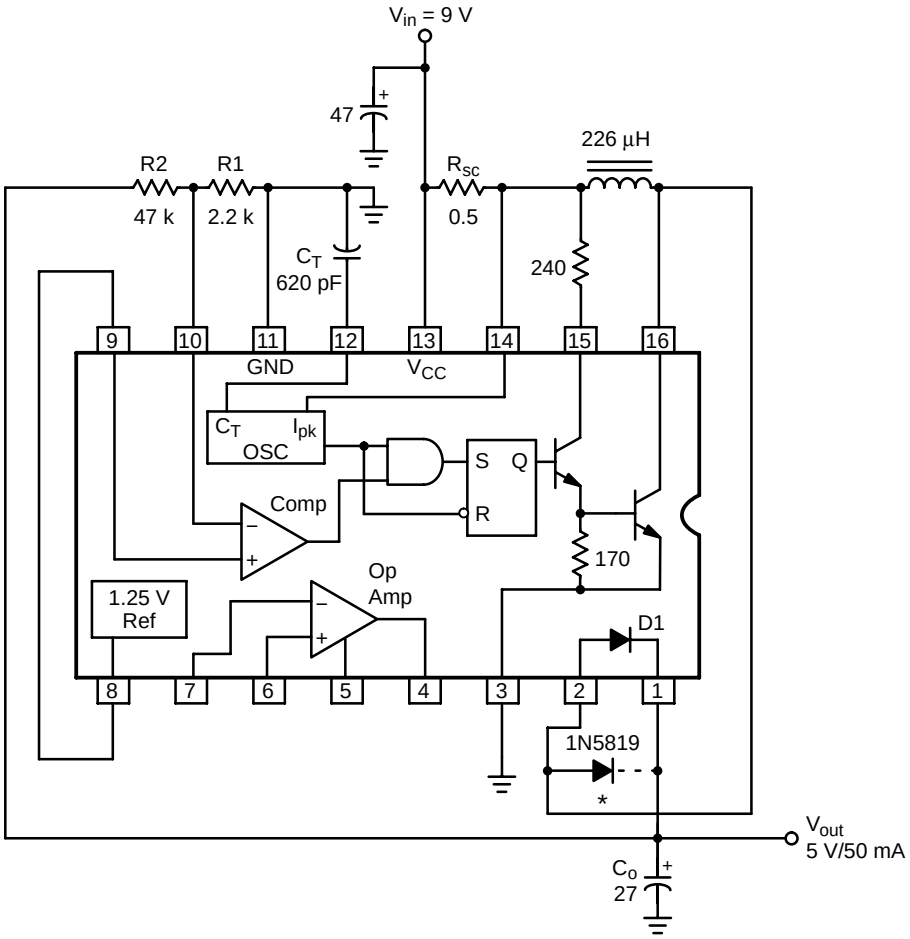
$$= 33.6 \text{ mV}$$

A 27 μF tantalum capacitor with an ESR of 0.10 Ω was again chosen. The ripple voltage due to the capacitance value is 28.7 mV and 44.2 mV due to ESR. This yields a total ripple voltage of:

$$E_{ripple(p-p)} = \frac{V_{out}}{V_{ref}} 1.5 \times 10^{-3} + \frac{I_{out}}{C_o} t_{on} + I_{pk} \text{ ESR}$$

$$= 33.6 \text{ mV} + 28.7 \text{ mV} + 44.2 \text{ mV}$$

$$= 107 \text{ mV}$$



Test	Conditions	Results
Line Regulation	V_{in} = 6.0 to 12 V, I_{out} = 50 mA	Δ = 120 mV or ± 0.21%
Load Regulation	V_{in} = 9.0 V, I_{out} = 25 to 50 mA	Δ = 50 mV or ± 0.09%
Output Ripple	V_{in} = 6.75 V, I_{out} = 50 mA	90 mV_{p-p}
Efficiency, Internal Diode	V_{in} = 9.0 V, I_{out} = 50 mA	62.2%
Efficiency, External Diode*	V_{in} = 9.0 V, I_{out} = 50 mA	74.2%

Figure 11. Step−Up Design Example

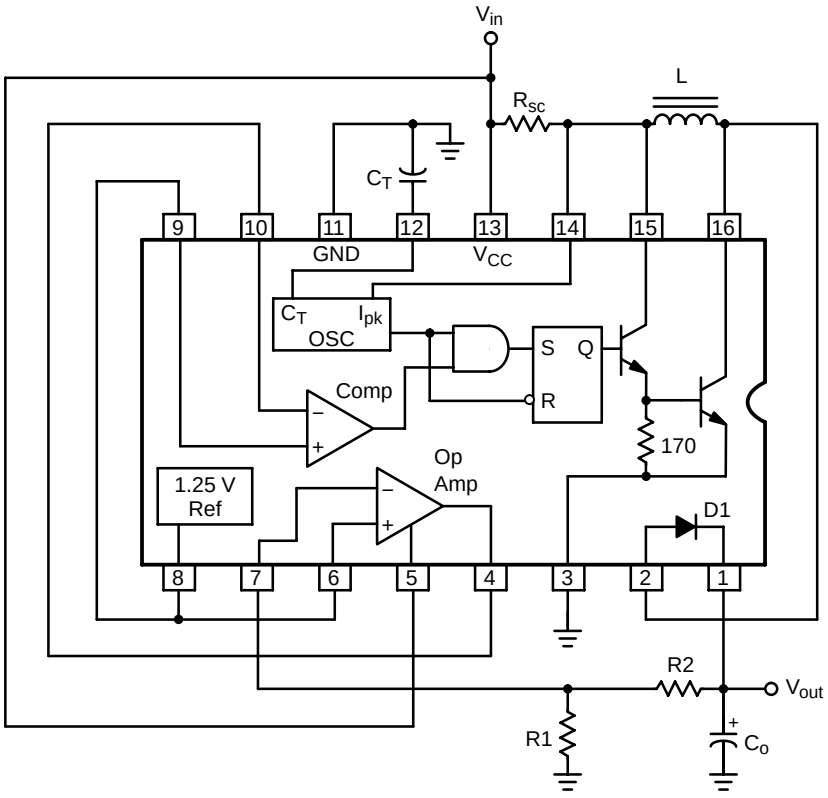


Figure 12. μA78S40 Ripple Reduction Technique

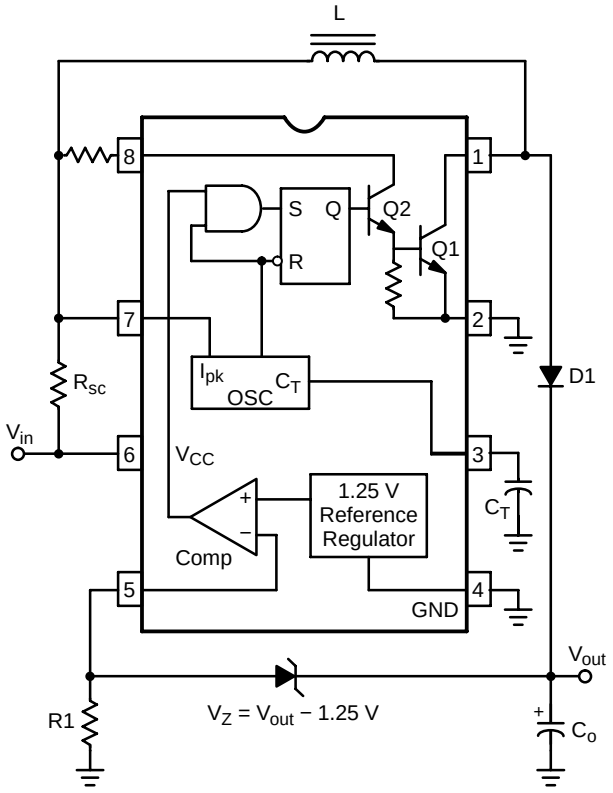


Figure 13. MC34063 Ripple Reduction Technique

9. The nominal output voltage is programmed by the R1, R2 divider.

$$V_{out} = 1.25\left(1 + \frac{R2}{R1}\right)$$

A standard 5% tolerance, 2.2 k resistor was selected for R1 so that the divider current is about 500 μA.

$$R1 = \frac{1.25}{500 \times 10^{-6}}$$

$$= 2500\ \Omega,\ \text{use } 2.2\ \text{k}$$

$$\text{Then}\quad R2 = R1\left(\frac{V_{out}}{1.25} - 1\right)$$

$$= 2200\left(\frac{28}{1.25} - 1\right)$$

$$= 47,080\ \Omega,\ \text{use } 47\ \text{k}$$

10. In this design example, the output switch transistor is driven into saturation with a forced gain of 20 at an input voltage of 7.0 V. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_f}$$

$$= \frac{442 \times 10^{-3}}{20}$$

$$= 22.1\ \text{mA}$$

The current required to drive the internal 170 Ω base−emitter resistor is:

$$I_{170\ \Omega} = \frac{V_{BE(switch)}}{170}$$

$$= \frac{0.7}{170}$$

$$= 4.1\ mA$$

The driver collector current is equal to sum of 22.1 mA + 4.1 mA = 26.2 mA. Allow 0.3 V for driver saturation and 0.2 V for the drop across R_{sc} (0.5 × 442 mA I_{pk}).

Then the driver collector resistor is equal to:

$$R_{driver} = \frac{V_{in} - V_{sat(driver)} - V_{RSC}}{I_B + I_{170\ \Omega}}$$

$$= \frac{7.0 - 0.3 - 0.2}{(22.1 + 4.1) \times 10^{-3}}$$

$$= 248\ \Omega,\ \text{use } 240\ \Omega$$

VOLTAGE−INVERTING SWITCHING REGULATOR OPERATION

The basic voltage−inverting switching regulator is shown in Figure 7c and the operating waveforms are in Figure 14. Energy is stored in the inductor during the conduction time of Q1. Upon turn−off, the energy is transferred to the output filter capacitor and load. Notice that in this configuration the output voltage is derived only from the inductor. This allows the magnitude of the output to be set to any value. It may be less than, equal to, or greater than that of the input and is set by the following relationship:

$$V_{out} = V_{in}\left(\frac{t_{on}}{t_{off}}\right)$$

The voltage−inverting converter operates almost identically to that of the step−up previously discussed. The voltage across the inductor during t_{on} is $V_{in} - V_{sat}$ but during t_{off} the voltage is equal to the negative magnitude of $V_{out} + V_F$. Remember that the volt−time product of t_{on} must be equal to that of t_{off}, a ratio of t_{on} to t_{off} can be determined.

$$(V_{in} - V_{sat})\ t_{on} = (|V_{out}| + V_F)\ t_{off}$$

$$\therefore \frac{t_{on}}{t_{off}} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}}$$

The derivations and the formulas for $I_{pk(switch)}$, L_{min}, and C_o are the same as that of the step−up converter.

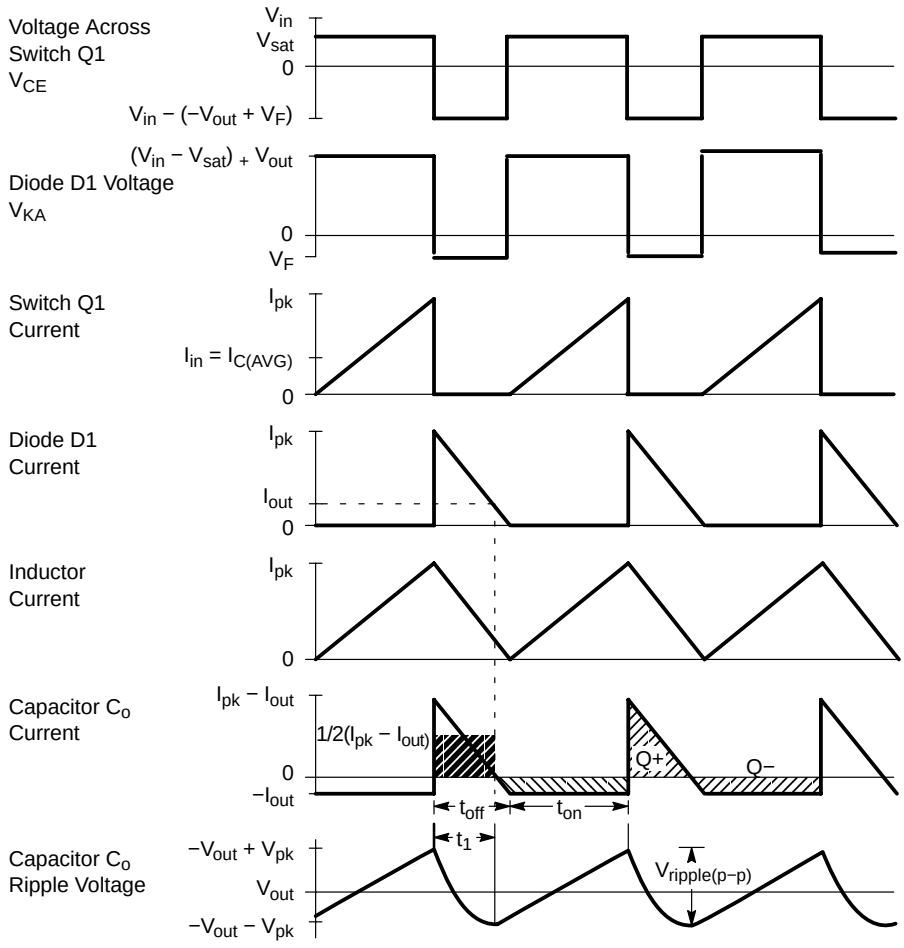


Figure 14. Voltage−Inverting Switching Regulator Waveforms

Voltage−Inverting Switching Regulator Design Example

A circuit diagram of the basic voltage−inverting regulator is shown in Figure 15.

The μA78S40 was selected for this design since it has the reference and both comparator inputs pinned out. The following operating conditions are given:

V_{out} = −15 V
I_{out} = 500 mA
f_{min} = 50 kHz
$V_{in(min)}$ = 15 V − 10% or 13.5 V
$V_{ripple(p-p)}$ = 0.4% V_{out} or 60 mV_{p-p}

1. Determine the ratio of switch conduction t_{on} versus diode conductions t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{|V_{out}| + V_F}{V_{in} - V_{sat}}$$

$$= \frac{15 + 0.8}{13.5 - 0.8}$$

$$= 1.24$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^{-3}}$$

$$= 20\ \mu s$$

3. Calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on} + t_{off}$ in #2.

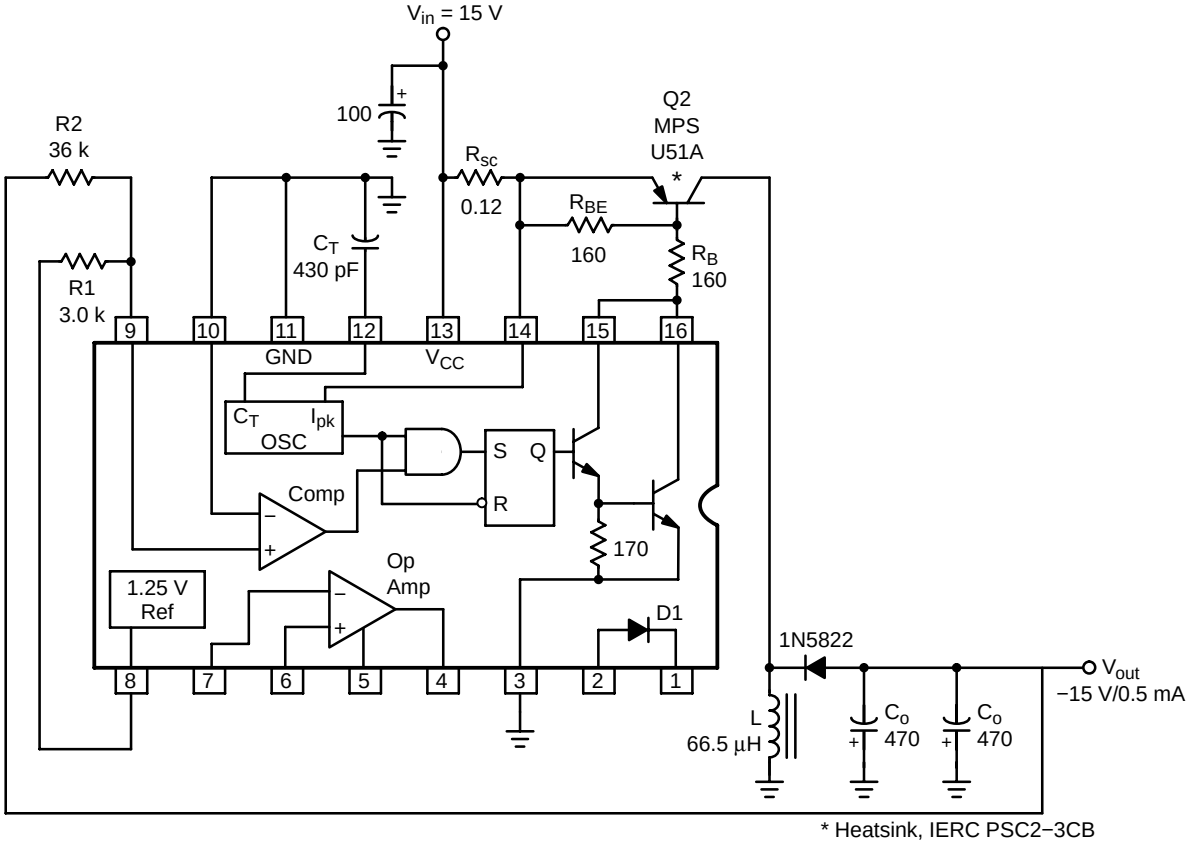
$$t_{off} = \frac{20 \times 10^{-6}}{1.24 + 1}$$

$$= 8.9\ \mu s$$

$$t_{on} = 20\ \mu s - 8.9\ \mu s$$

$$= 11.1\ \mu s$$

Note again that the ratio of $t_{on}/(t_{on} + t_{off})$ does not exceed the maximum of 0.857.



Test	Conditions	Results
Line Regulation	V_{in} = 12 to 16 V, I_{out} = 0.5 A	Δ = 3.0 mV or ± 0.01%
Load Regulation	V_{in} = 15 V, I_{out} = 0.1 to 0.5 A	Δ = 27 mV or ± 0.09%
Output Ripple	V_{in} = 13.5 V, I_{out} = 0.5 A	35 mV_{p-p}
Short Circuit Current	V_{in} = 15 V, R_L = 0.1 Ω	2.5 A
Efficiency	V_{in} = 15 V, I_{out} = 0.5 A	80.6%

Figure 15. Voltage−Inverting Design Example

4. A value of C_T must be selected in order to set $t_{on(max)}$.

$$C_T = 4.0 \times 10^{-5}\, t_{on}$$
$$= 4.0 \times 10^{-5}\, (11.1 \times 10^{-6})$$
$$= 444\ \text{pF},\ \text{use } 430\ \text{pF}$$

5. The peak switch current is:

$$I_{pk(switch)} = 2\, I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$
$$= 2\, (500 \times 10^{-3})\, (1.24 + 1)$$
$$= 2.24\ \text{A}$$

6. The minimum required inductance value is:

$$L_{min} = \left(\frac{V_{in(min)} - V_{sat}}{I_{pk(switch)}}\right) t_{on}$$
$$= \left(\frac{13.5 - 0.8}{2.24}\right) 11.1 \times 10^{-6}$$
$$= 66.5\ \mu\text{H}$$

7. The current−limit resistor value was selected by determining the level of $I_{pk(switch)}$ for V_{in} = 16.5 V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{sat}}{L_{min}}\right) t_{on}$$
$$= \left(\frac{16.5 - 0.8}{66.5 \times 10^{-6}}\right) 11.1 \times 10^{-6}$$
$$= 2.62\ \text{A}$$
$$R_{SC} = \frac{0.33}{I'_{pk(switch)}}$$
$$= \frac{0.33}{2.62}$$
$$= 0.13\ \Omega,\ \text{use } 0.12\ \Omega$$

8. An approximate value for an ideal output filter capacitor is:

$$C_O \approx \left(\frac{I_{out}}{V_{ripple(p-p)}}\right) t_{on}$$
$$\approx \frac{0.5}{60 \times 10^{-3}}\, 11.1 \times 10^{-6}$$
$$\approx 92.5\ \mu\text{F}$$

The ripple contribution due to the gain of the comparator is:

$$V_{ripple(p-p)} = \frac{|V_{out}|}{V_{ref}}\, 1.5 \times 10^{-3}$$
$$= \frac{15}{1.25}\, 1.5 \times 10^{-3}$$
$$= 18\ \text{mV}$$

For a given level of ripple, the ESR of the output filter capacitor becomes the dominant factor in choosing a value for capacitance. Therefore two 470 μF capacitors with an ESR of 0.020 Ω each was chosen. The ripple voltage due to the capacitance value is 5.9 mV and 22.4 mV due to ESR. This yields a total ripple voltage of:

$$E_{ripple(p-p)} = \frac{|V_{out}|}{V_{ref}}\, 1.5 \times 10^{-3} + \frac{I_{out}}{C_O}\, t_{on} + I_{pk}\, ESR$$
$$= 18\ \text{mV} + 5.9\ \text{mV} + 22.4\ \text{mV}$$
$$= 46.3\ \text{mV}$$

9. The nominal output voltage is programmed by the R1, R2 divider. Note that with a negative output voltage, the inverting input of the comparator is referenced to ground. Therefore, the voltage at the junction of R1, R2 and the noninverting input must also be at ground potential when V_{out} is in regulation. The magnitude of V_{out} is:

$$|V_{out}| = 1.25\, \frac{R2}{R1}$$

A divider current of about 400 μA was desired for this example.

$$R1 = \frac{1.25}{400 \times 10^{-6}}$$
$$= 3{,}125\ \Omega,\ \text{use } 3.0\ \text{k}$$

$$\text{Then}\quad R2 = \frac{|V_{out}|}{1.25}\, R1$$
$$= \frac{15}{1.25}\, 3.0 \times 10^{-3}$$
$$= 36\ \text{k}$$

10. Output switch transistor Q2 is driven into a soft saturation with a forced gain of 35 at an input voltage of 13.5 V in order to enhance the turn−off switching time. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_f}$$
$$= \frac{2.24}{35}$$
$$= 64\ \text{mA}$$

The value for the base−emitter turn−off resistor R_{BE} is determined by:

$$R_{BE} = \frac{10\, B_f}{I_{pk(switch)}}$$
$$= \frac{10\ (35)}{2.24}$$
$$= 156.3\ \Omega,\ \text{use } 160\ \Omega$$

The additional base current required due to R_{BE} is:

$$I_{R_{BE}} = \frac{V_{BE}\ (Q2)}{R_{BE}}$$
$$= \frac{0.8}{160}$$
$$= 5.0\ \text{mA}$$

Then I_B (Q2) is equal to the sum of 64 mA + 5.0 mA = 69 mA. Allow 0.8 V for the IC driver saturation and 0.3 V for the drop across R_{sc} (0.12×2.24 A I_{pk}). Then the base driver resistor is equal to:

$$R_B = \frac{V_{in(min)} - V_{sat(IC)} - V_{RSC} - V_{BE(Q2)}}{I_B + I_{160\ \Omega}}$$

$$= \frac{13.5 - 0.8 - 0.3 - 1.0}{(64 + 5) \times 10^{-3}}$$

$$= 165.2\ \Omega,\ \text{use } 160\ \Omega$$

STEP UP/DOWN SWITCHING REGULATOR OPERATION

When designing at the board level it sometimes becomes necessary to generate a constant output voltage that is less than that of the battery. The step−down circuit shown in Figure 16a will perform this function efficiently. However, as the battery discharges, its terminal voltage will eventually fall below the desired output, and in order to utilize the remaining battery energy the step−up circuit shown in Figure 16b will be required.

General Applications

By combining circuits a and b, a unique step−up/down configuration can be created (Figure 17) which still employs a *simple inductor* for the voltage transformation. Energy is stored in the inductor during the time that transistors Q1 and Q2 are in the "on" state. Upon turn−off, the energy is transferred to the output filter capacitor and load forward biasing diodes D1 and D2. Note that during t_{on} this circuit is identical to the basic step−up, but during t_{off} the output voltage is derived only from the inductor and is with respect to ground instead of V_{in}. This allows the output voltage to be set to any value, thus it may be less than, equal to, or greater than that of the input. Current limit protection cannot be employed in the basic step−up circuit. If the output is severely overloaded or shorted, L or D2 may be destroyed since they form a direct path from V_{in} to V_{out}. The step−up/down configuration allows the control circuit to implement current limiting because Q1 is now in series with V_{out}, as is in the step−down circuit.

Step−Up/Down Switching Regulator Design Example

A complete step−up/down switching regulator design example is shown in Figure 18. An external switch transistor was used to perform the function of Q2. This regulator was designed to operate from a standard 12 V battery pack with the following conditions:

V_{in} = 7.5 to 14.5 V
V_{out} = 10 V
f_{min} = 50 kHz
I_{out} = 120 mA
$V_{ripple(p-p)}$ = 1% V_{out} or 100 mV_{p-p}

The following design procedure is provided so that the user can select proper component values for his specific converter application.

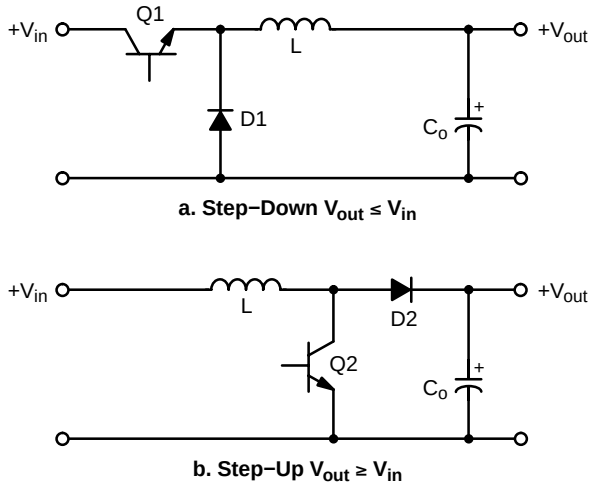


Figure 16. Basic Switching Regulator Configurations

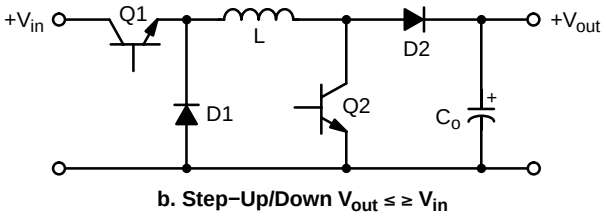


Figure 17. Combined Configuration

1. Determine the ratio of switch conduction t_{on} versus diode conduction t_{off} time.

$$\frac{t_{on}}{t_{off}} = \frac{V_{out} + V_{FD1} + V_{FD2}}{V_{in(min)} - V_{satQ1} - V_{satQ2}}$$

$$= \frac{10 + 0.6 + 0.6}{7.5 - 0.8 - 0.8}$$

$$= 1.9$$

2. The cycle time of the LC network is equal to $t_{on(max)} + t_{off}$.

$$t_{on(max)} + t_{off} = \frac{1}{f_{min}}$$

$$= \frac{1}{50 \times 10^3}$$

$$= 20\ \mu s \text{ per cycle}$$

3. Next calculate t_{on} and t_{off} from the ratio of t_{on}/t_{off} in #1 and the sum of $t_{on(max)} + t_{off}$ in #2.

$$t_{off} = \frac{t_{on(max)} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$$

$$= \frac{20 \times 10^{-6}}{1.9 + 1}$$

$$= 6.9\ \mu s$$

$$t_{on} = 20\ \mu s - 6.9\ \mu s$$

$$= 13.1\ \mu s$$

4. The maximum on−time is set by selecting a value for C_T.

$$C_T = 4.0 \times 10^{-5}\, t_{on(max)}$$
$$= 4.0 \times 10^{-5}\,(13.1 \times 10^{-6})$$
$$= 524\ pF$$

Use a standard 510 pF capacitor.

5. The peak switch current is:

$$I_{pk(switch)} = 2\, I_{out}\left(\frac{t_{on}}{t_{off}} + 1\right)$$
$$= 2\,(120 \times 10^{-3})\,(1.9 + 1)$$
$$= 696\ mA$$

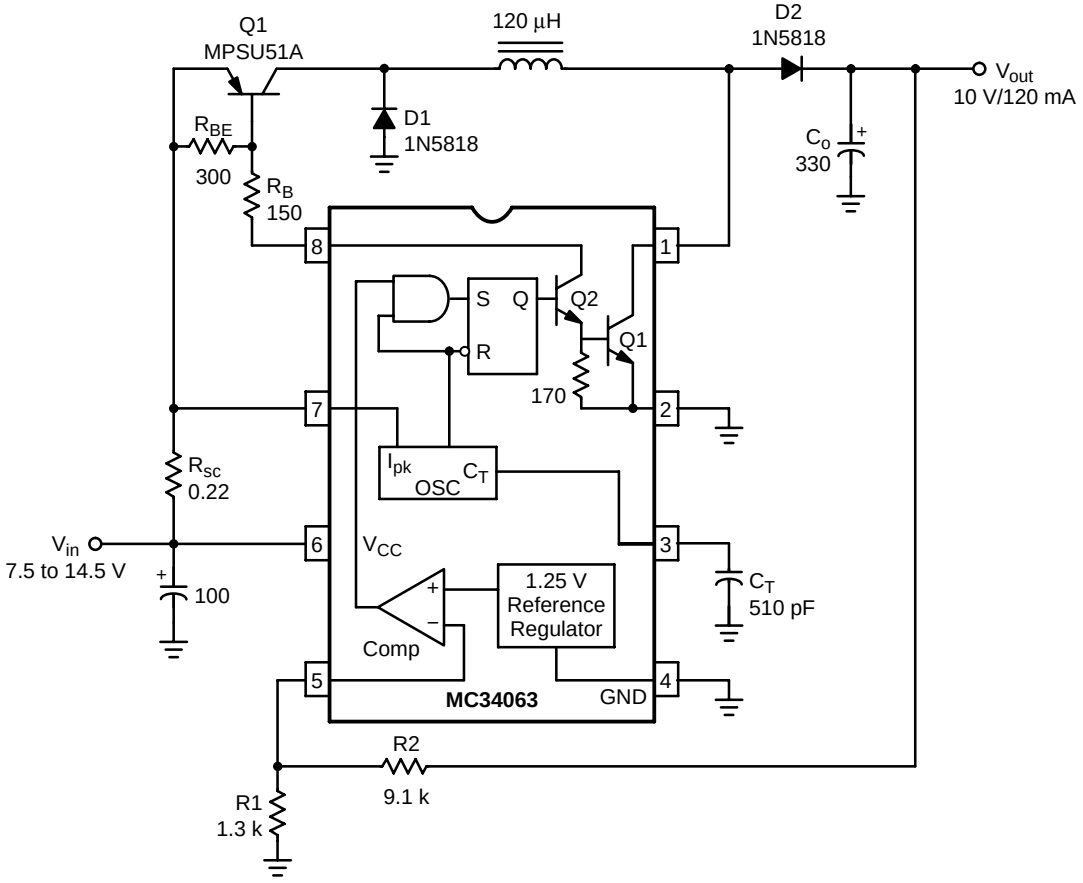
6. A minimum value of inductance can now be calculated since the maximum on−time and peak switch current are known.

$$L_{min} = \left(\frac{V_{in(min)} - V_{satQ1} - V_{satQ2}}{I_{pk(switch)}}\right) t_{on}$$
$$= \left(\frac{7.5 - 0.8 - 0.8}{696 \times 10^{-3}}\right) 13.1 \times 10^{-6}$$
$$= 111\ \mu H$$

A 120 μH inductor was selected for L_{min}.

7. A value for the current limit resistor, R_{sc}, can be determined by using the current limit level of $I_{pk(switch)}$ when V_{in} = 14.5 V.

$$I'_{pk(switch)} = \left(\frac{V_{in} - V_{satQ1} - V_{satQ2}}{L_{min}}\right) t_{on(max)}$$
$$= \left(\frac{14.5 - 0.8 - 0.8}{120 \times 10^{-6}}\right) 13.1 \times 10^{-6}$$
$$= 1.41\ A$$



Test	Conditions	Results
Line Regulation	V_{in} = 7.5 to 14.5 V, I_{out} = 120 mA	Δ = 22 mV or ± 0.11%
Load Regulation	V_{in} = 12.6 V, I_{out} = 10 to 120 mA	Δ = 3.0 mV or ± 0.015%
Output Ripple	V_{in} = 12.6 V, I_{out} = 120 mA	95 mV_{p-p}
Short Circuit Current	V_{in} = 12.6 V, R_L = 0.1 Ω	1.54 A
Efficiency	V_{in} = 7.5 to 14.5 V, I_{out} = 120 mA	74%

Figure 18. Step−Up/Down Switching Regulator Design Example

$$R_{sc} = \frac{0.33}{I'_{pk(switch)}}$$

$$= \frac{0.33}{1.41}$$

$$= 0.23\ \Omega$$

Use a standard 0.22 Ω resistor.

8. A minimum value for an *ideal* output filter capacitor is:

$$C_o \approx \left(\frac{I_{out}}{V_{ripple(p-p)}}\right) t_{on}$$

$$\approx \left(\frac{120 \times 10^{-3}}{100 \times 10^{-3}}\right) 13.1 \times 10^{-6}$$

$$\approx 15.7\ \mu F$$

Ideally this would satisfy the design goal, however, even a solid tantalum capacitor of this value will have a typical ESR (equivalent series resistance) of 0.3 Ω which will contribute an additional 209 mV of ripple. Also there is a ripple component due to the gain of the comparator equal to:

$$V_{ripple(p-p)} = \left(\frac{V_{out}}{V_{ref}}\right) 1.5 \times 10^{-3}$$

$$= \left(\frac{10}{1.25}\right) 1.5 \times 10^{-3}$$

$$= 12\ mV$$

The ripple components are not in phase, but can be assumed to be for a conservative design. From the above it becomes apparent that ESR is the dominant factor in the selection of an output filter capacitor. A 330 μF with an ESR of 0.12 Ω was selected to satisfy this design example by the following:

$$ESR \approx \frac{V_{ripple(p-p)} - \left(\frac{I_{out}}{C_o}\right) t_{on} - \left(\frac{V_{out}}{V_{Ref}}\right) 1.5 \times 10^{-3}}{I_{pk(switch)}}$$

9. The nominal output voltage is programmed by the R1, R2 resistor divider.

$$R2 = R1\left(\frac{V_{out}}{V_{Ref}} - 1\right)$$

$$= R1\left(\frac{10}{1.25} - 1\right)$$

$$= 7\ R1$$

If 1.3 k is chosen for R1, then R2 would be 9.1 k, both being standard resistor values.

10. Transistor Q1 is driven into saturation with a forced gain of approximately 20 at an input voltage of 7.5 V. The required base drive is:

$$I_B = \frac{I_{pk(switch)}}{B_f}$$

$$= \frac{696 \times 10^{-3}}{20}$$

$$= 35\ mA$$

The value for the base−emitter turn−off resistor R_{BE} is determined by:

$$R_{BE} = \frac{10\ B_f}{I_{pk(switch)}}$$

$$= \frac{10\ (20)}{696 \times 10^{-3}}$$

$$= 287\ \Omega$$

A standard 300 Ω resistor was selected.

The additional base current required due to R_{BE} is:

$$I_{R_{BE}} = \frac{V_{BEQ1}}{R_{BE}}$$

$$= \frac{0.8}{300}$$

$$= 3.0\ mA$$

The base drive resistor for Q1 is equal to:

$$R_B = \frac{V_{in(min)} - V_{sat(driver)} - V_{RSC} - V_{BEQ1}}{I_B + I_{R_{BE}}}$$

$$= \frac{7.5 - 0.8 - 0.15 - 0.8}{(35 + 3) \times 10^{-3}}$$

$$= 151\ \Omega$$

A standard 150 Ω resistor was used.

The circuit performance data shows excellent line and load regulation. There is some loss in conversion efficiency over the basic step−up or step−down circuits due to the added switch transistor and diode “on” losses. However, this unique converter demonstrates that with a simple inductor, a step−up/down converter with current limiting can be constructed.

DESIGN CONSIDERATIONS

As perviously stated, the design equations for L_{min} were based upon the assumption that the switching regulator is operating on the onset of continuous conduction with a fixed input voltage, maximum output load current, and a minimum charge−current oscillator. Typically the oscillator charge−current will be greater than the specific minimum of 20 microamps, thus t_{on} will be somewhat shorter and the actual LC operating frequency will be greater than predicted.

Also note that the voltage drop developed across the current−limit resistor R_{sc} was not accounted for in the t_{on}/t_{off} and L_{min} design formulas. This voltage drop must be considered when designing high current converters that operate with an input voltage of less than 5.0 V.

When checking the initial switcher operation with an oscilloscope, there will be some concern of circuit instability due to the apparent random switching of the output. The oscilloscope will be difficult to synchronize. This is not a problem. It is a normal operating characteristic of this type of switching regulator and is caused by the asynchronous operation of the comparator to that of the oscillator. The oscilloscope may be synchronized by varying the input voltage or load current slightly from the design nominals.

High frequency circuit layout techniques are imperative with switching regulators. To minimize EMI, all high current loops should be kept as short as possible using heavy copper runs. The low current signal and high current switch and output grounds should return on separate paths back to the input filter capacitor. The R1, R2 output voltage divider should be located as close to the IC as possible to eliminate any noise pick−up into the feedback loop. The circuit diagrams were purposely drawn in a manner to depict this.

All circuits used molypermalloy power toroid cores for the magnetics where only the inductance value is given. The number of turns, wire and core size information is not given since no attempt was made to optimize their design. Inductor and transformer design information may be obtained from the magnetic core and assembly companies listed on the switching regulator component source table.

In some circuit designs, mainly step−up and voltage−inverting, a ratio of $t_{on}/(t_{on} + t_{off})$ greater than 0.857 may be required. This can be obtained by the addition of the ratio extender circuit shown in Figure 19. This circuit uses germanium components and is temperature sensitive. A negative temperature coefficient timing capacitor will help reduce this sensitivity. Figure 20 shows the output switch on and off time versus C_T with and without the ratio extender circuit. Notice that without the circuit, the ratio of $t_{on}/(t_{on} + t_{off})$ is limited to 0.857 only for values of C_T greater than 2.0 nF. With the circuit, the ratio is variable depending upon the value chosen for C_T since t_{off} is now nearly a constant. Current limiting must be used on all step−up and voltage−inverting designs using the ratio extender circuit. This will allow the inductor time to reset between cycles of overcurrent during initial power up of the switcher. When the output filter capacitor reaches its nominal voltage, the voltage feedback loop will control regulation.

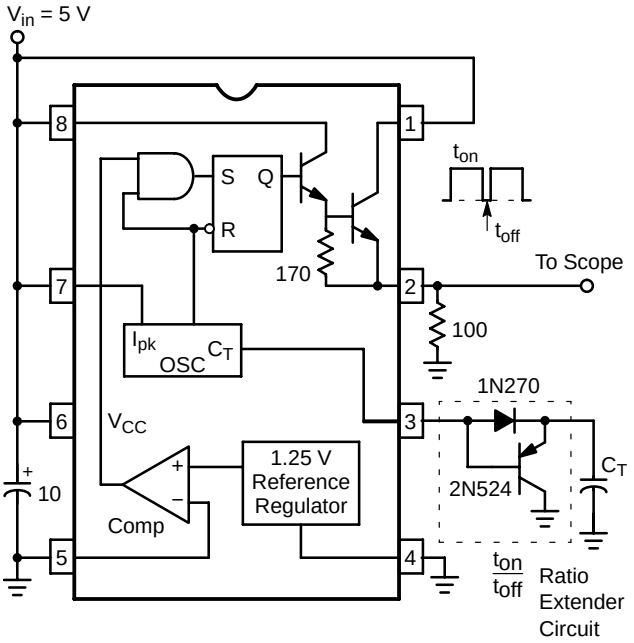


Figure 19. Output Switch On−Off Time Test Circuit

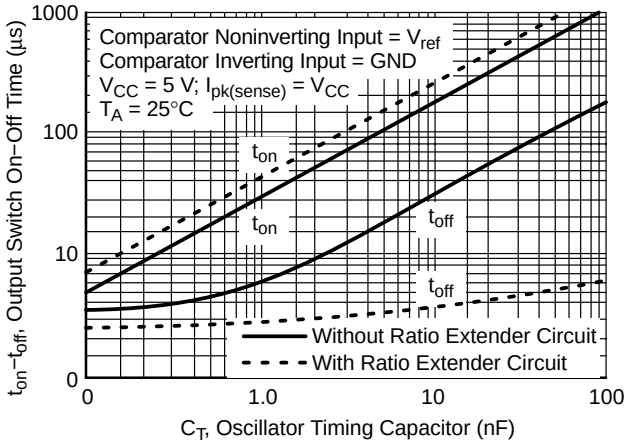


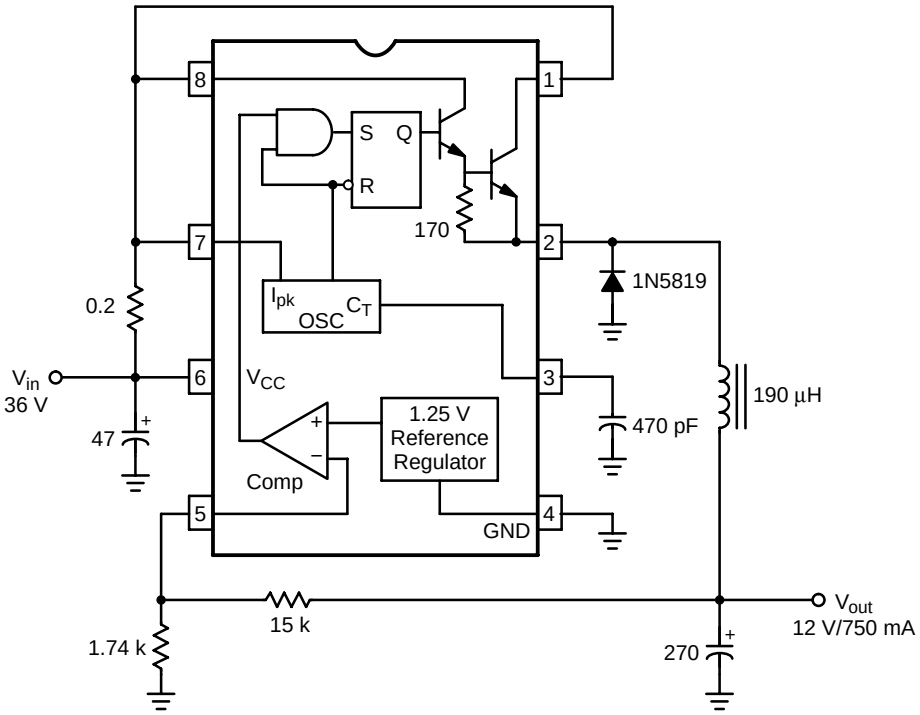
Figure 20. Output Switch On−Off Time versus Oscillator Timing Capacitor

APPLICATIONS SECTION

Listed below is an index of all the converter circuits shown in this application note. They are categorized into three major groups based upon the main output configuration. Each of these circuits was constructed and tested, and a performance table is included.

INDEX OF CONVERTER CIRCUITS

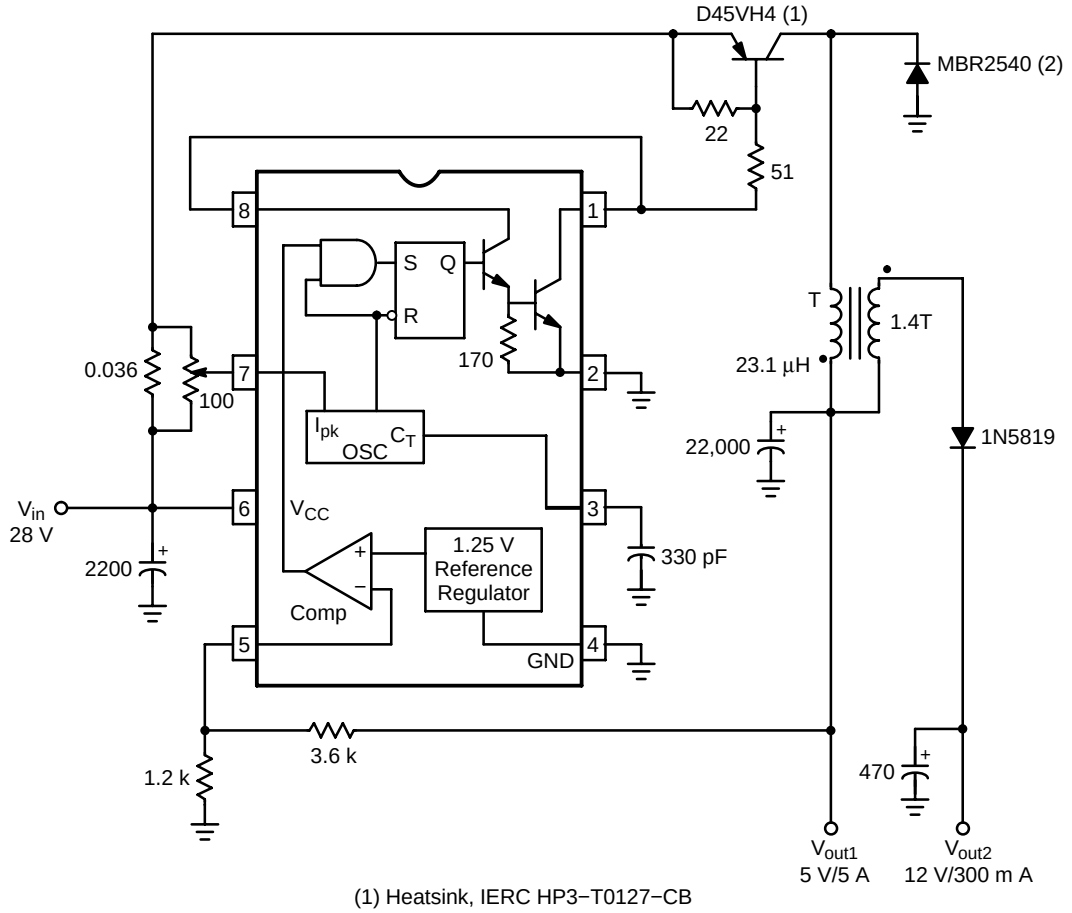
Main Output Configuration		Input V	Output 1 V/mA	Output 2 V/mA	Output 3 V/mA	Figure No.
Step−Down						
µA78S40	Low Power with Minimum Components	24	5/50	−	−	9
MC34063	Medium Power	36	12/750	−	−	21
MC34063	Buffered Switch and Second Output	28	5.0/5000	12/300	−	22
µA78S40	Linear Pass from Main Output	33	24/500	15/50	−	23
µA78S40	Buffered Switch and Buffered Linear Pass from Main Output	28	15/3000	12/1000	−	24
µA78S40	Negative Input and Negative Output	−28	−12/500	−	−	25
Step−Up						
µA78S40	Low Power with Minimum Components	9.0	28/50	−	−	11
MC34063	Medium Power	12	36/225	−	−	26
MC34063	High Voltage, Low Power	4.5	190/5.0	−	−	27
µA78S40	High Voltage, Medium Power Photoflash	4.5	334/45	−	−	28
µA78S40	Linear Pass from Main Output	2.5	9.0/100	6/30	−	29
µA78S40	Buffered Linear Pass from Main Output EE PROM Programmer	4.5	See Circuit	−	−	30
µA78S40	Buffered Switch and Buffered Linear Pass from Main Output	4.5	15/1000	12/500	−12/50	31
µA78S40	Dual Switcher, Step−Up and Step−Down with Buffered Switch	12	28/250	5.0/250	−	32
Step−Up/Down						
MC34063	Medium Power Step−Up/Down	7.5 to 14.5	10/120	−	−	18
Voltage−Inverting						
MC34063	Low Power	5.0	−12/100	−	−	33
µA78S40	Medium Power with Buffered Switch	15	−15/500	−	−	15
µA78S40	High Voltage, High Power with Buffered Switch	28	−120/850	−	−	34
µA78S40	42 Watt Off−Line Flyback Switcher	115 Vac	5.0/4000	12/700	−12/700	35
µA78S40	Tracking Regulator with Buffered Switch and Buffered Linear Pass from Input	15	−12/500	12/500	−	37



Test	Conditions	Results
Line Regulation	V_{in} = 20 to 40 V, I_{out} = 750 mA	Δ = 15 mV or ± 0.063%
Load Regulation	V_{in} = 36 V, I_{out} = 100 to 750 mA	Δ = 40 mV or ± 0.17%
Output Ripple	V_{in} = 36 V, I_{out} = 750 mA	60 mV_{p-p}
Short Circuit Current	V_{in} = 36 V, R_L = 0.1 Ω	1.6 A
Efficiency	V_{in} = 36 V, I_{out} = 750 mA	89.5%

A maximum power transfer of 9.0 watts is possible from an 8−pin dual−in−line package with V_{in} = 36 V and V_{out} = 12 V.

Figure 21. Step−Down

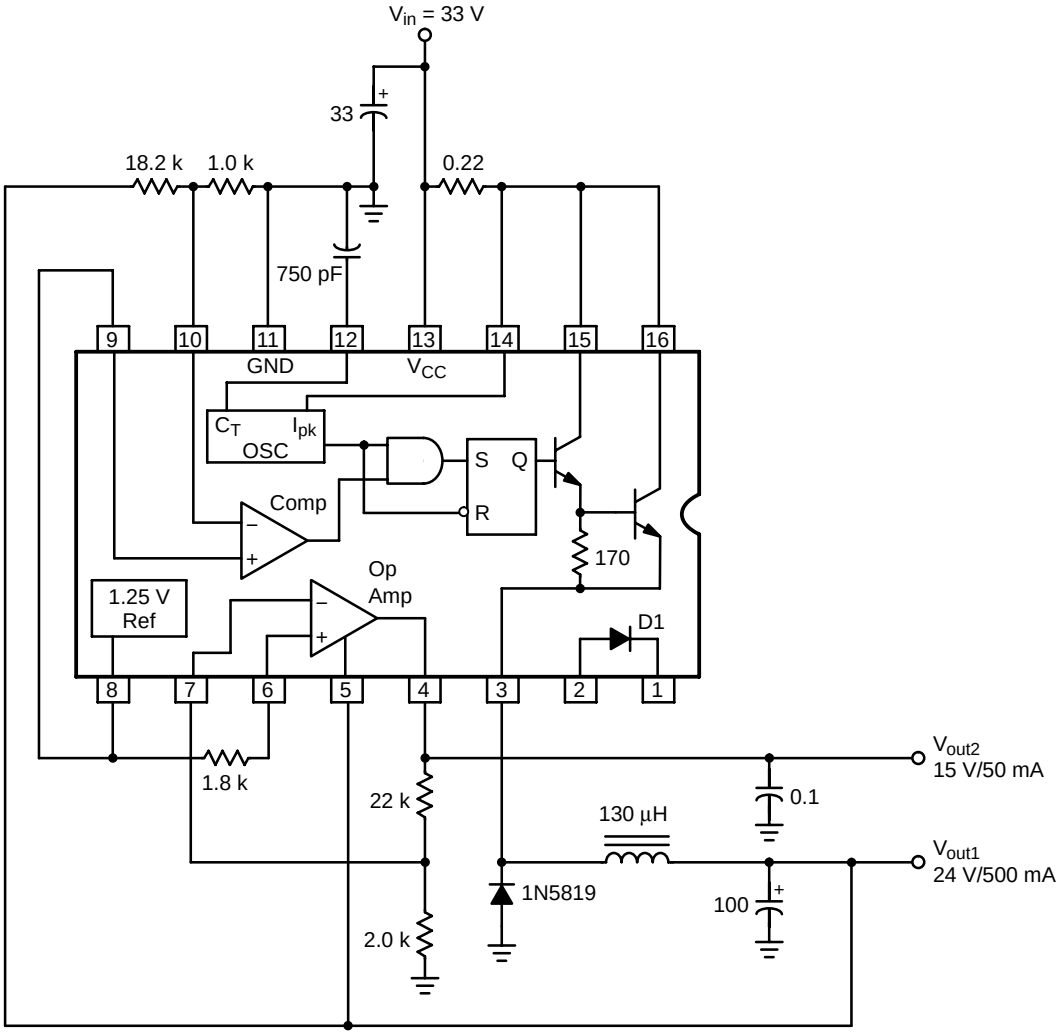


(1) Heatsink, IERC HP3−T0127−CB
(2) Heatsink, IERC UP−000−CB

Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 20 to 30 V, I_{out1} = 5.0 A, I_{out2} = 300 mA	Δ = 9.0 mV or ± 0.09%
Load Regulation	V_{out1}	V_{in} = 28 V, I_{out1} = 1.0 to 5.0 A, I_{out2} = 300 mA	Δ = 20 mV or ± 0.2%
Output Ripple	V_{out1}	V_{in} = 28 V, I_{out1} = 5.0 A, I_{out2} = 300 mA	60 mV_{p-p}
Short Circuit Current	V_{out1}	V_{in} = 28 V, R_L = 0.1 Ω	11.4 A
Line Regulation	V_{out2}	V_{in} = 20 to 30 V, I_{out1} = 5.0 A, I_{out2} = 300 mA	Δ = 72 mV or ± 0.3%
Load Regulation	V_{out2}	V_{in} = 20 V, I_{out2} = 100 to 300 mA, I_{out1} = 5.0 A	Δ = 12 mV or ± 0.05%
Output Ripple	V_{out2}	V_{in} = 28 V, I_{out1} = 5.0 A, I_{out2} = 300 mA	25 mV_{p-p}
Short Circuit Current	V_{out2}	V_{in} = 28 V, R_L = 0.1 Ω	11.25 A
Efficiency		V_{in} = 28 V, I_{out1} = 5.0 A, I_{out2} = 300 mA	80%

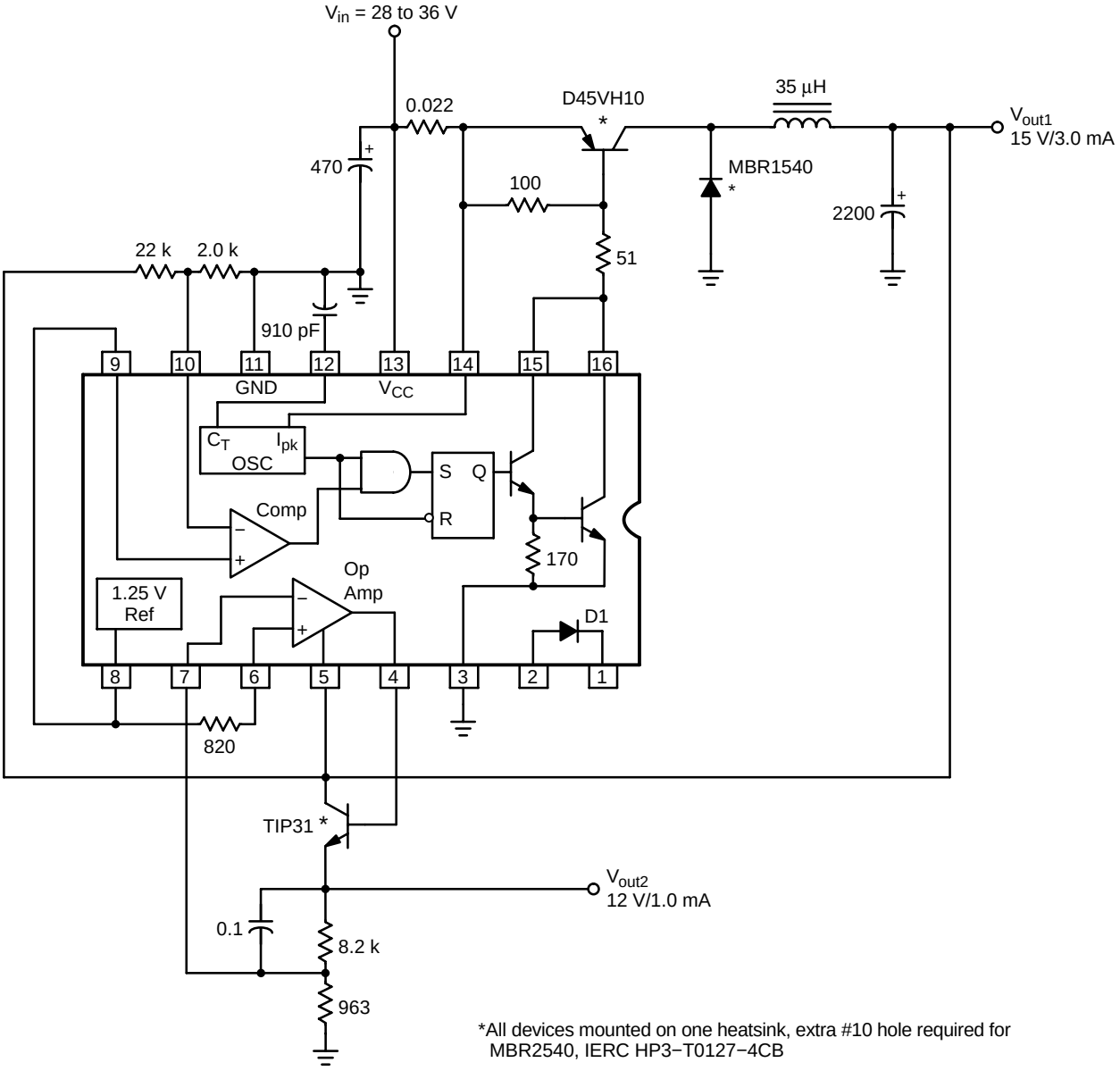
A second output can be easily derived by winding a secondary on the main output inductor and phasing it so that energy is delivered to V_{out2} during t_{off}. The second output power should not exceed 25% of the main output. The 100 Ω potentiometer is used to divide down the voltage across the 0.036 Ω resistor and thus fine tune the current limit.

Figure 22. Step−Down with Buffered Switch and Second Output



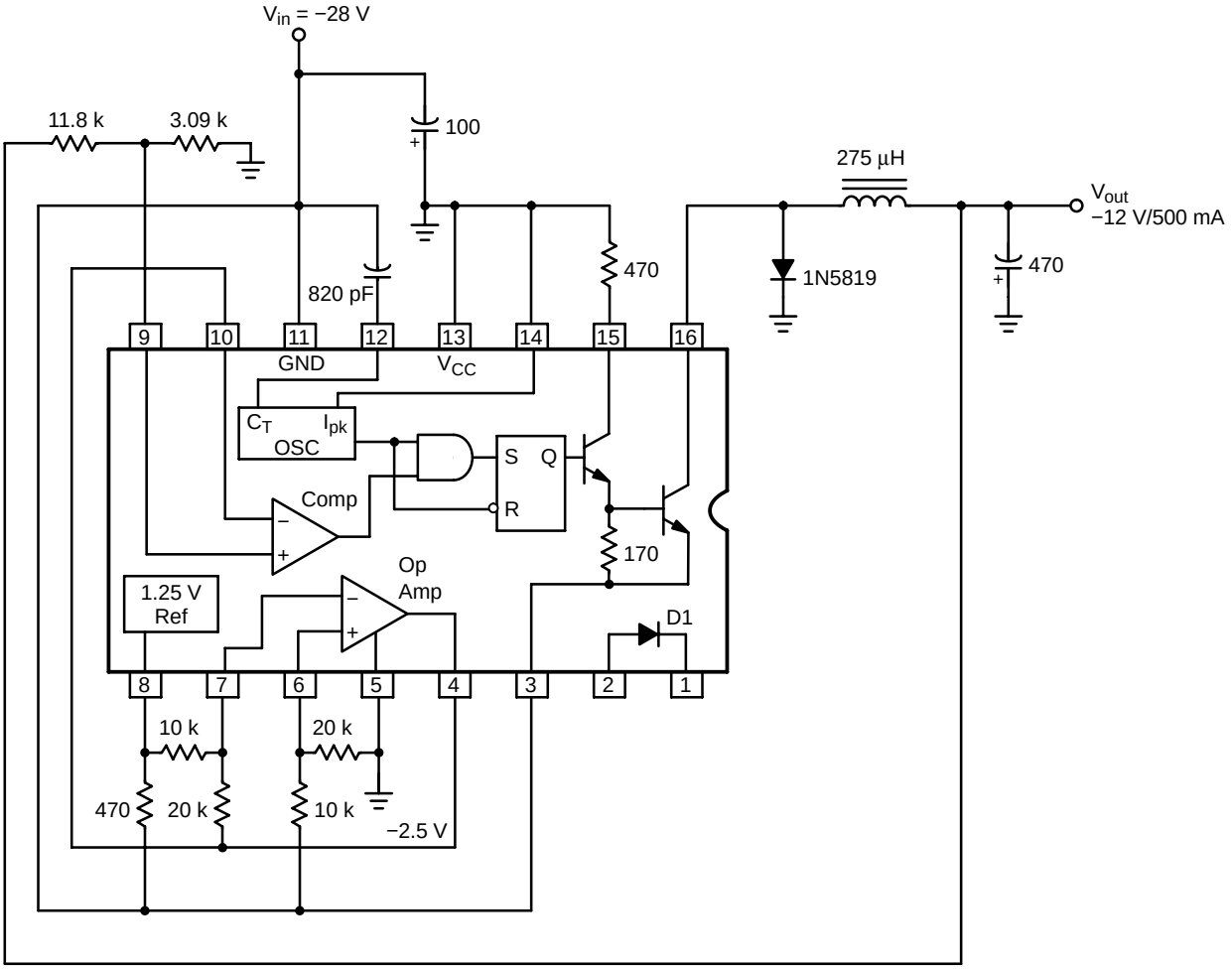
Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 30 to 36 V, I_{out1} = 500 mA, I_{out2} = 50 mA	Δ = 30 mV or ± 0.63%
Load Regulation	V_{out1}	V_{in} = 33 V, I_{out1} = 100 to 500 mA, I_{out2} = 50 mA	Δ = 70 mV or ± 0.15%
Output Ripple	V_{out1}	V_{in} = 33 V, I_{out1} = 500 mA, I_{out2} = 50 mA	80 mV_{p-p}
Short Circuit Current	V_{out1}	V_{in} = 33 V, R_L = 0.1 Ω	2.5 A
Line Regulation	V_{out2}	V_{in} = 30 to 36 V, I_{out1} = 500 mA, I_{out2} = 50 mA	Δ = 20 mV or ± 0.067%
Load Regulation	V_{out2}	V_{in} = 33 V, I_{out2} = 0 to 50 mA, I_{out1} = 500 mA	Δ = 60 mV or ± 0.2%
Output Ripple	V_{out2}	V_{in} = 33 V, I_{out1} = 500 mA, I_{out2} = 50 mA	70 mV_{p-p}
Short Circuit Current	V_{out2}	V_{in} = 33 V, R_L = 0.1 Ω	90 mA
Efficiency		V_{in} = 33 V, I_{out1} = 500 mA, I_{out2} = 50 mA	88.2%

Figure 23. Step−Down with Linear Pass from Main Output



Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 28 to 36 V, I_{out1} = 3.0 A, I_{out2} = 1.0 A	Δ = 13 mV or ± 0.043%
Load Regulation	V_{out1}	V_{in} = 36 V, I_{out1} = 1.0 to 4.0 A, I_{out2} = 1.0 A	Δ = 21 mV or ± 0.07%
Output Ripple	V_{out1}	V_{in} = 36 V, I_{out1} = 3.0 mA, I_{out2} = 1.0 A	120 mV_{p-p}
Short Circuit Current	V_{out1}	V_{in} = 36 V, R_L = 0.1 Ω	12.6 A
Line Regulation	V_{out2}	V_{in} = 28 to 36 V, I_{out1} = 3.0 A, I_{out2} = 1.0 A	Δ = 2.0 mV or ± 0.008%
Load Regulation	V_{out2}	V_{in} = 36 V, I_{out2} = 0 to 1.5 A	Δ = 2.0 mV or ± 0.08%
Output Ripple	V_{out2}	V_{in} = 36 V, I_{out1} = 3.0 A, I_{out2} = 1.0 A	25 mV_{p-p}
Short Circuit Current	V_{out2}	V_{in} = 36 V, R_L = 0.1 Ω	3.6 A
Efficiency		V_{in} = 36 V, I_{out1} = 3.0 A, I_{out2} = 1.0 A	78.5%

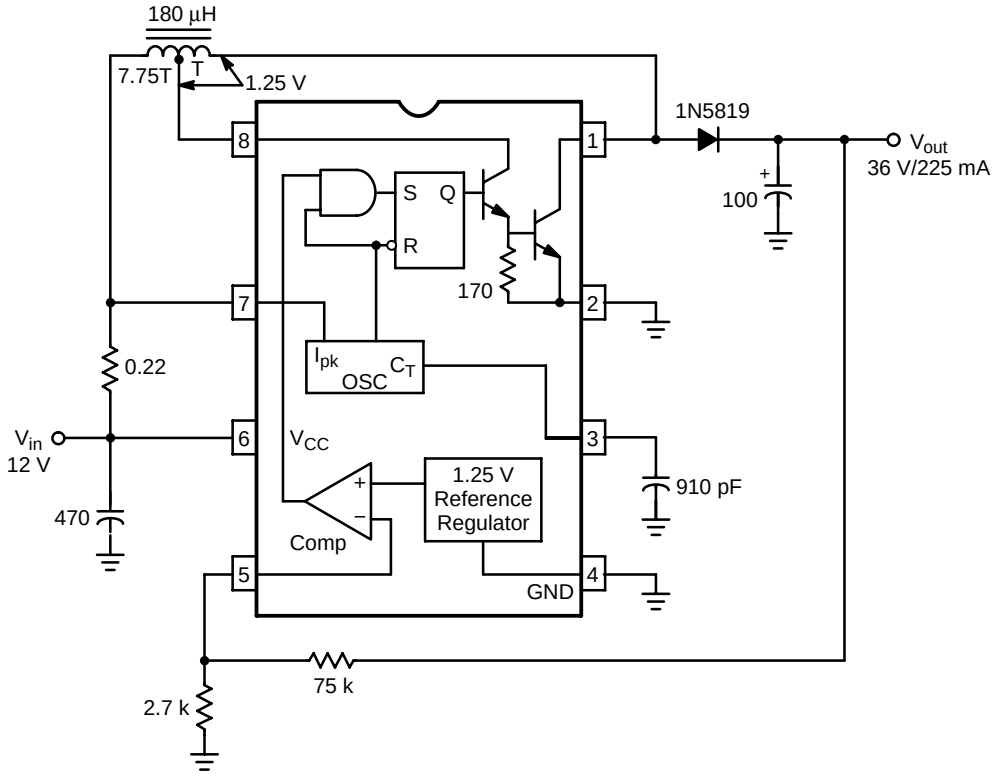
Figure 24. Step−Down with Buffered Switch and Buffered Linear Pass from Main Output



Test	Conditions	Results
Line Regulation	V_{in} = −22 to −28 V, I_{out} = 500 mA	Δ = 25 mV or ± 0.104%
Load Regulation	V_{in} = −28 V, I_{out} = 100 to 500 mA	Δ = 10 mV or ± 0.042%
Output Ripple	V_{in} = −28 V, I_{out} = 500 mA	130 mV_{p-p}
Efficiency	V_{in} = −28 V, I_{out} = 500 mA	85.5%

In this step−down circuit, the output switch must be connected in series with the negative input, causing the internal 1.25 V reference to be with respect to $-V_{in}$. A second reference of −2.5 V with respect to ground is generated by the Op Amp. Note that the 10 k and 20 k resistors must be matched pairs for good line regulation and that no provision is made for output short−circuit protection.

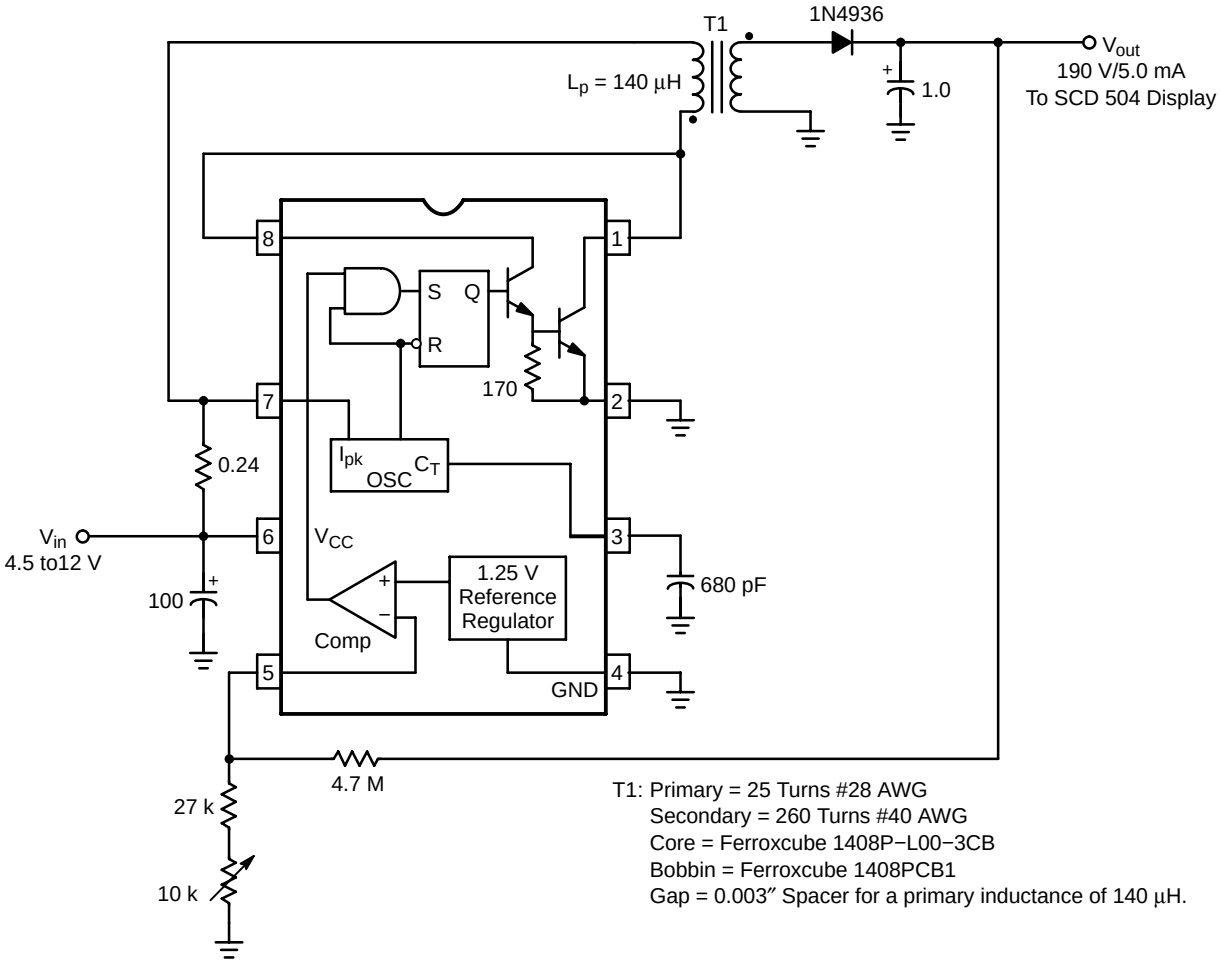
Figure 25. Step−Down with Negative Input and Negative Output



Test	Conditions	Results
Line Regulation	V_{in} = 11 to 15 V, I_{out} = 225 mA	Δ = 20 mV or ± 0.028%
Load Regulation	V_{in} = 12 V, I_{out} = 50 to 225 mA	Δ = 30 mV or ± 0.042%
Output Ripple	V_{in} = 12 V, I_{out} = 225 mA	100 mV_{p-p}
Efficiency	V_{in} = 12 V, I_{out} = 225 mA	90.4%

A maximum power transfer of 8.1 watts is possible with V_{in} = 12 V and V_{out} = 36 V. The high efficiency is partially due to the use of the tapped inductor. The tap point is set for a voltage differential of 1.25 V. The range of V_{in} is somewhat limited when using this method.

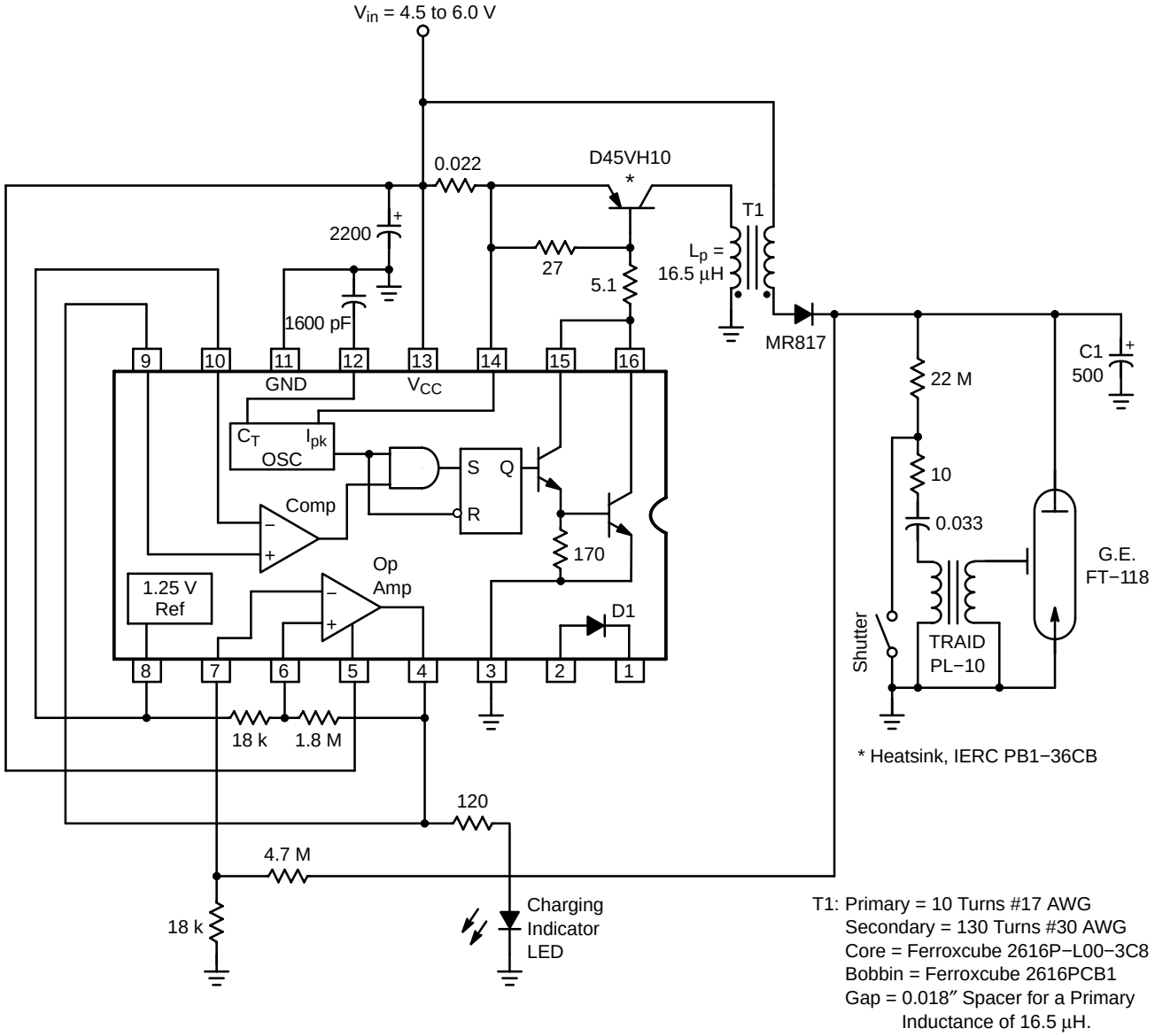
Figure 26. Step−Up



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 to 12 V, I_{out} = 5.0 mA	Δ = 2.3 V or ± 0.61%
Load Regulation	V_{in} = 5.0 V, I_{out} = 1.0 to 6.0 mA	Δ = 1.4 V or ± 0.37%
Output Ripple	V_{in} = 5.0 V, I_{out} = 5.0 mA	250 mV_{p-p}
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	113 mA
Efficiency	V_{in} = 5.0 V, I_{out} = 5.0 mA	68%

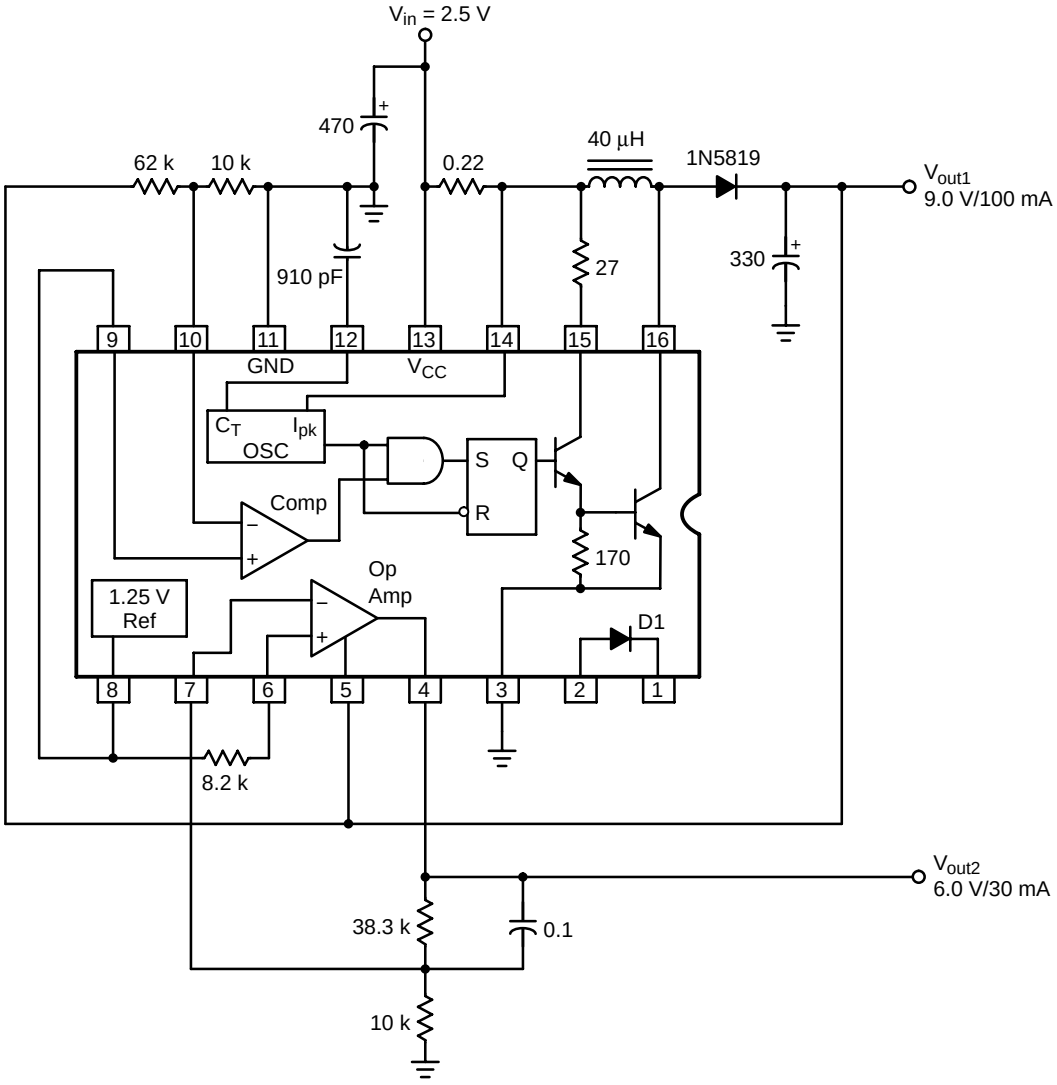
This circuit was designed to power the ON Semiconductor Solid Ceramic Displays from a V_{in} of 4.5 to 12 V. The design calculations are based on a step−up converter with an input of 4.5 V and a 24 V output rated at 45 mA. The 24 V level is the maximum step−up allowed by the oscillator ratio of $t_{on}/(t_{on} + t_{off})$. The 45 mA current level was chosen so that the transformer primary power level is about 10% greater than that required by the load. The maximum V_{in} of 12 V is determined by the sum of the flyback and leakage inductance voltages present at the collector of the output switch during turn−off must not exceed 40 V.

Figure 27. High−Voltage, Low Power Step−Up for Solid Ceramic Display



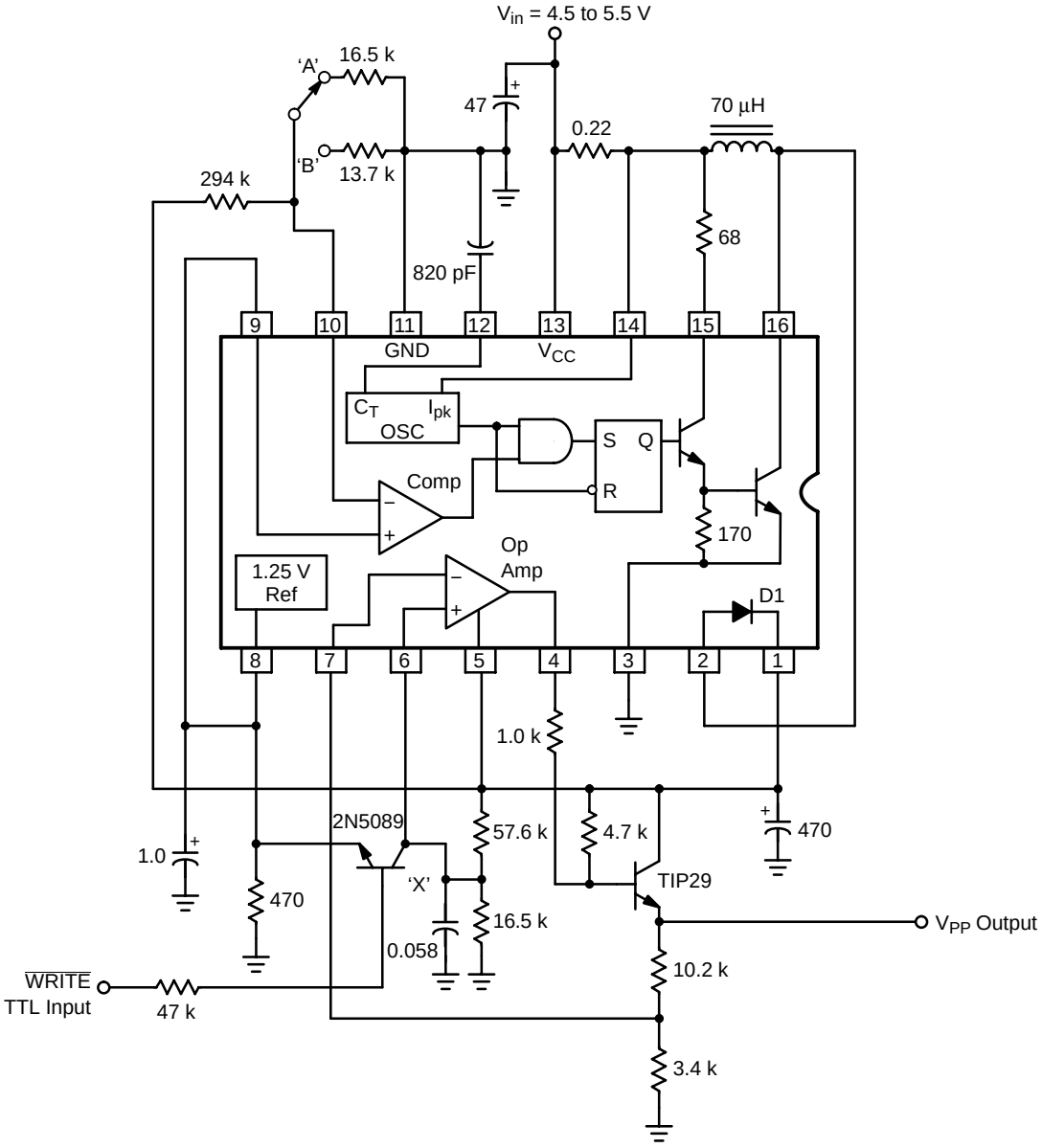
With V_{in} of 6.0 V, this step−up converter will charge capacitor C1 from 0 to 334 V in 4.7 seconds. The switching operation will cease until C1 bleeds down to 323 V. The charging time between flashes is 4.0 seconds. The output current at 334 V is 45 mA.

Figure 28. High−Voltage Step−Up with Buffered Switch for Photoflash Applications



Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 2.5 to 3.5 V, I_{out1} = 100 mA, I_{out2} = 30 mA	Δ = 20 mV or ± 0.11%
Load Regulation	V_{out1}	V_{in} = 2.5 V, I_{out1} = 25 to 100 mA, I_{out2} = 30 mA	Δ = 20 mV or ± 0.11%
Output Ripple	V_{out1}	V_{in} = 2.5 V, I_{out1} = 100 mA, I_{out2} = 30 mA	60 mV_{p-p}
Line Regulation	V_{out2}	V_{in} = 2.5 to 3.5 V, I_{out1} = 100 mA, I_{out2} = 30 mA	Δ = 1.0 mV or ± 0.0083%
Load Regulation	V_{out2}	V_{in} = 2.5 V, I_{out2} = 0 to 50 mA, I_{out1} = 100 mA	Δ = 1.0 mV or ± 0.0083%
Output Ripple	V_{out2}	V_{in} = 2.5 V, I_{out1} = 100 mA, I_{out2} = 30 mA	5.0 mV_{p-p}
Short Circuit Current	V_{out2}	V_{in} = 2.5 V, R_L = 0.1 Ω	150 mA
Efficiency		V_{in} = 3.0 V, I_{out1} = 100 mA, I_{out2} = 30 mA	68.3%

Figure 29. Step−Up with Linear Pass from Main Output

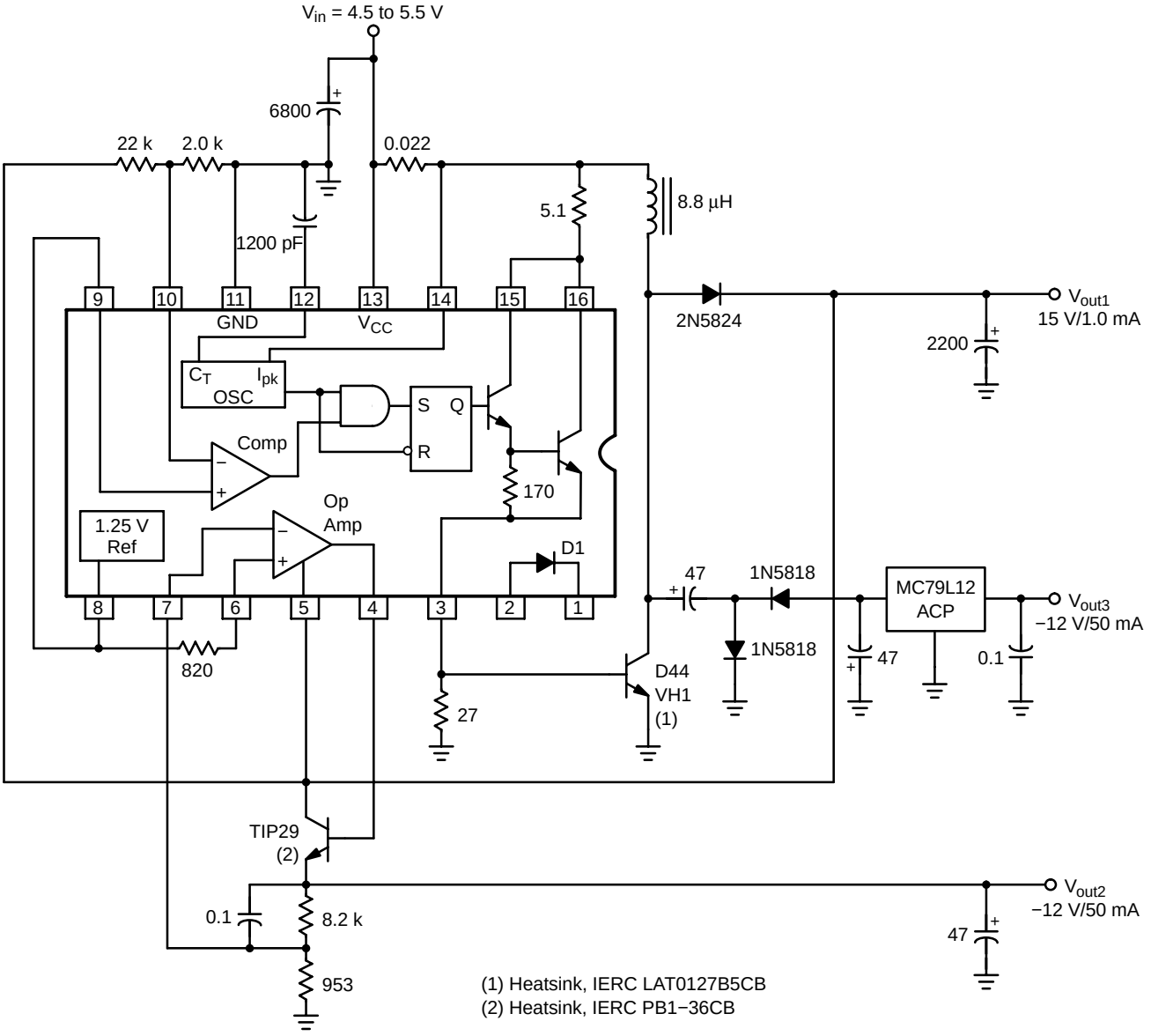


Switch Position	WRITE	Voltage @		
		Pins 1 & 5	X	V_{PP}
A	< 1.5	23.52	5.24	20.95
A	> 2.25	23.52	1.28	5.12
B	< 1.5	28.07	6.25	25.01
B	> 2.25	28.07	1.28	5.12

NOTE: All values are in volts. V_{ref} = 1.245 V. Contributed by Steve Hageman of Calex Mfg. Co. Inc.

Used in conjunction with two transistors, the µA78S40 can generate the required V_{PP} voltage of 21 V or 25 V needed to program and erase EEPROMs from a single 5.0 V supply. A step−up converter provides a selectable regulated voltage at Pins 1 and 5. This voltage is used to generate a second reference at point 'X' and to power the linear regulator consisting of the internal op amp and a TIP29 transistor. When the $\overline{\text{WRITE}}$ input is less than 1.5 V, the 2N5089 transistor is OFF, allowing the voltage at 'X' to rise exponentially with an approximate time constant of 600 µs as required by some EEPROMs. The linear regulator amplifies the voltage at 'X' by four, generating the required V_{PP} output voltage for the byte−erase write cycle. When the $\overline{\text{WRITE}}$ input is greater than 2.25 V, the 2N5089 turns ON clamping point 'X' to the internal reference level of 1.245 V. The V_{PP} output will not be at approximately 5.1 V or 4.0 (1.245 + V_{sat} 2N5089). The µA78AS40 reference can only source current, therefore a reference pre bias of 470 Ω is used. The V_{PP} output is short−circuit protected and can supply a current of 100 mA at 21 V or 75 mA at 25 V over an input range of 4.5 to 5.5 V.

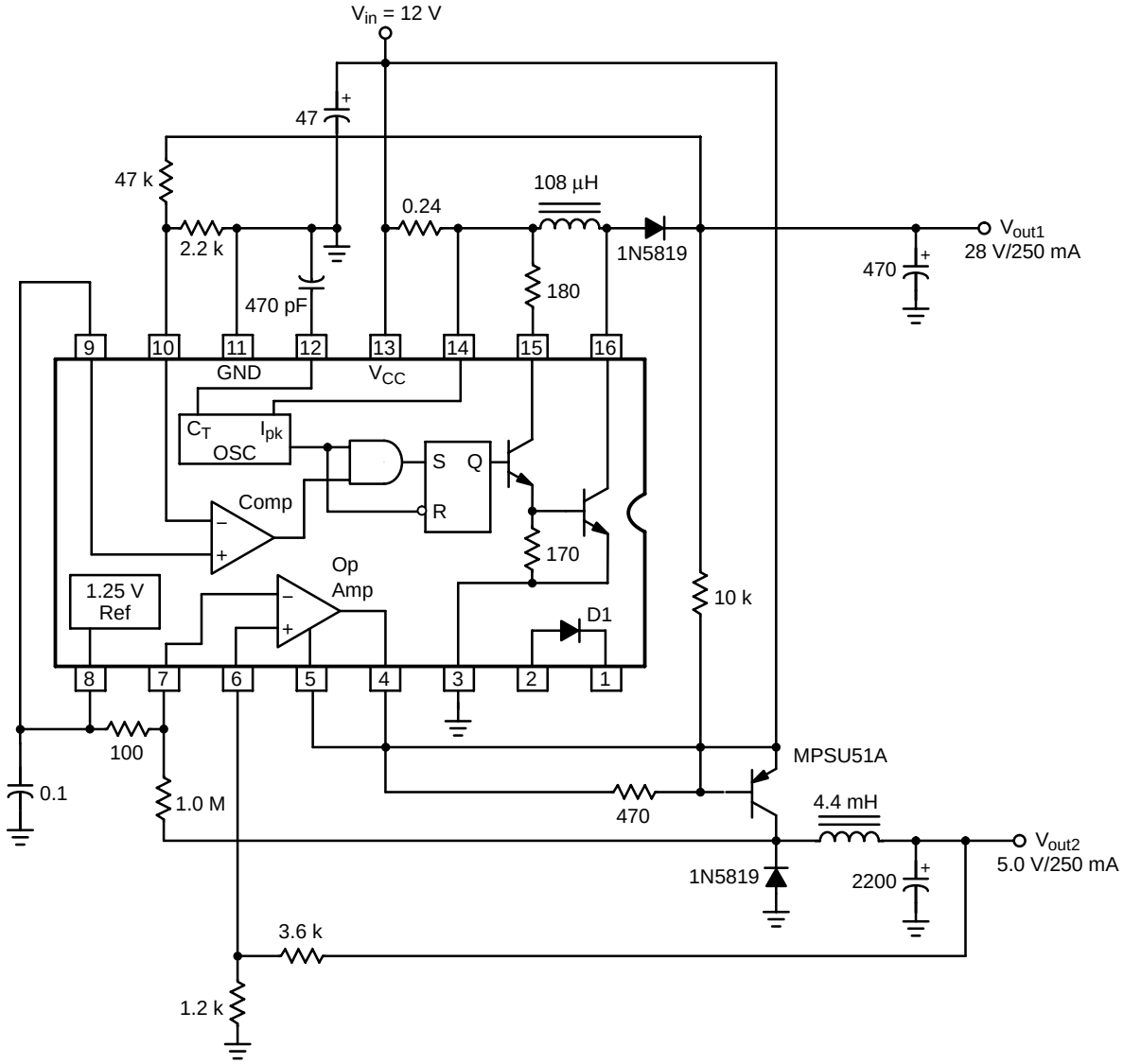
Figure 30. Step−Up with Buffered Linear Pass from Main Output for Programming EEPROMs



Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 4.5 to 5.5 V	Δ = 18 mV or ± 0.06%
Load Regulation	V_{out1}	V_{in} = 5.0 V, I_{out1} = 0.25 to 1.0 A	Δ = 25 mV or ± 0.083%
Output Ripple	V_{out1}	V_{in} = 5.0 V	75 mV_{p-p}
Line Regulation	V_{out2}	V_{in} = 4.5 to 5.5 V	Δ = 3.0 mV or ± 0.013%
Load Regulation	V_{out2}	V_{in} = 5.0 V, I_{out2} = 100 to 500 mA	Δ = 5.0 mV or ± 0.021%
Output Ripple	V_{out2}	V_{in} = 5.0 V	20 mV_{p-p}
Short Circuit Current	V_{out2}	V_{in} = 5.0 V, R_L = 0.1 Ω	2.7 A
Line Regulation	V_{out3}	V_{in} = 4.5 to 5.5 V	Δ = 2.0 mV or ± 0.008%
Load Regulation	V_{out3}	V_{in} = 5.0 V, I_{out3} = 0 to 50 mA	Δ = 29 mV or ± 0.12%
Output Ripple	V_{out3}	V_{in} = 5.0 V	15 mV_{p-p}
Short Circuit Current	V_{out3}	V_{in} = 5.0 V, R_L = 0.1 Ω	130 mA
Efficiency		V_{in} = 5.0 V	71.8%

NOTE: All outputs are at nominal load current unless otherwise noted.

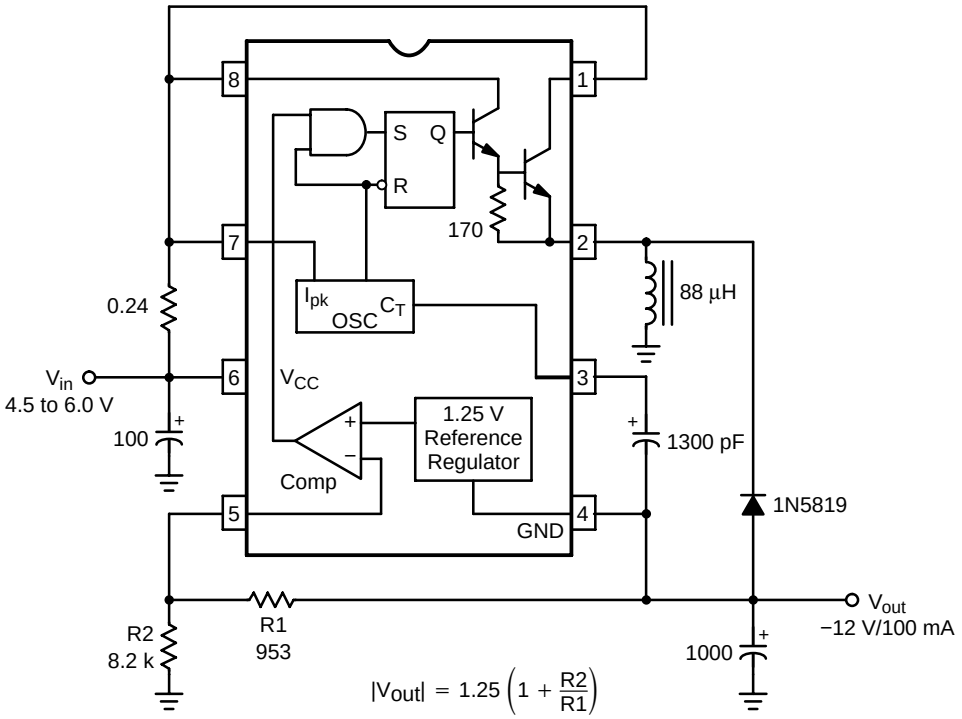
Figure 31. Step−Up with Buffered Switch and Buffered Linear Pass from Main Output



Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 9.0 to 15 V, I_{out1} = 250 mA, I_{out2} = 250 mA	Δ = 30 mV or ± 0.054%
Load Regulation	V_{out1}	V_{in} = 12 V, I_{out1} = 100 to 300 mA, I_{out2} = 250 mA	Δ = 20 mV or ± 0.036%
Output Ripple	V_{out1}	V_{in} = 12 V, I_{out1} = 250 mA, I_{out2} = 250 mA	35 mV_{p-p}
Short Circuit Current	V_{out1}	V_{in} = 12 V, R_L = 0.1 Ω	1.7 A
Line Regulation	V_{out2}	V_{in} = 9.0 to 15 V, I_{out1} = 250 mA, I_{out2} = 250 mA	Δ = 4.0 mV or ± 0.04%
Load Regulation	V_{out2}	V_{in} = 12 V, I_{out2} = 100 to 300 mA, I_{out1} = 250 A	Δ = 18 mV or ± 0.18%
Output Ripple	V_{out2}	V_{in} = 12 V, I_{out1} = 250 mA, I_{out2} = 250 mA	70 mV_{p-p}
Efficiency		V_{in} = 12 V, I_{out1} = 250 mA, I_{out2} = 250 mA	81.8%

This circuit shows a method of using the μA78S40 to construct two independent converters. Output 1 uses the typical step−up circuit configuration while Output 2 makes the use of the op amp connected with positive feedback to create a free running step−down converter. The op amp slew rate limits the maximum switching frequency at rated load to less than 2.0 kHz.

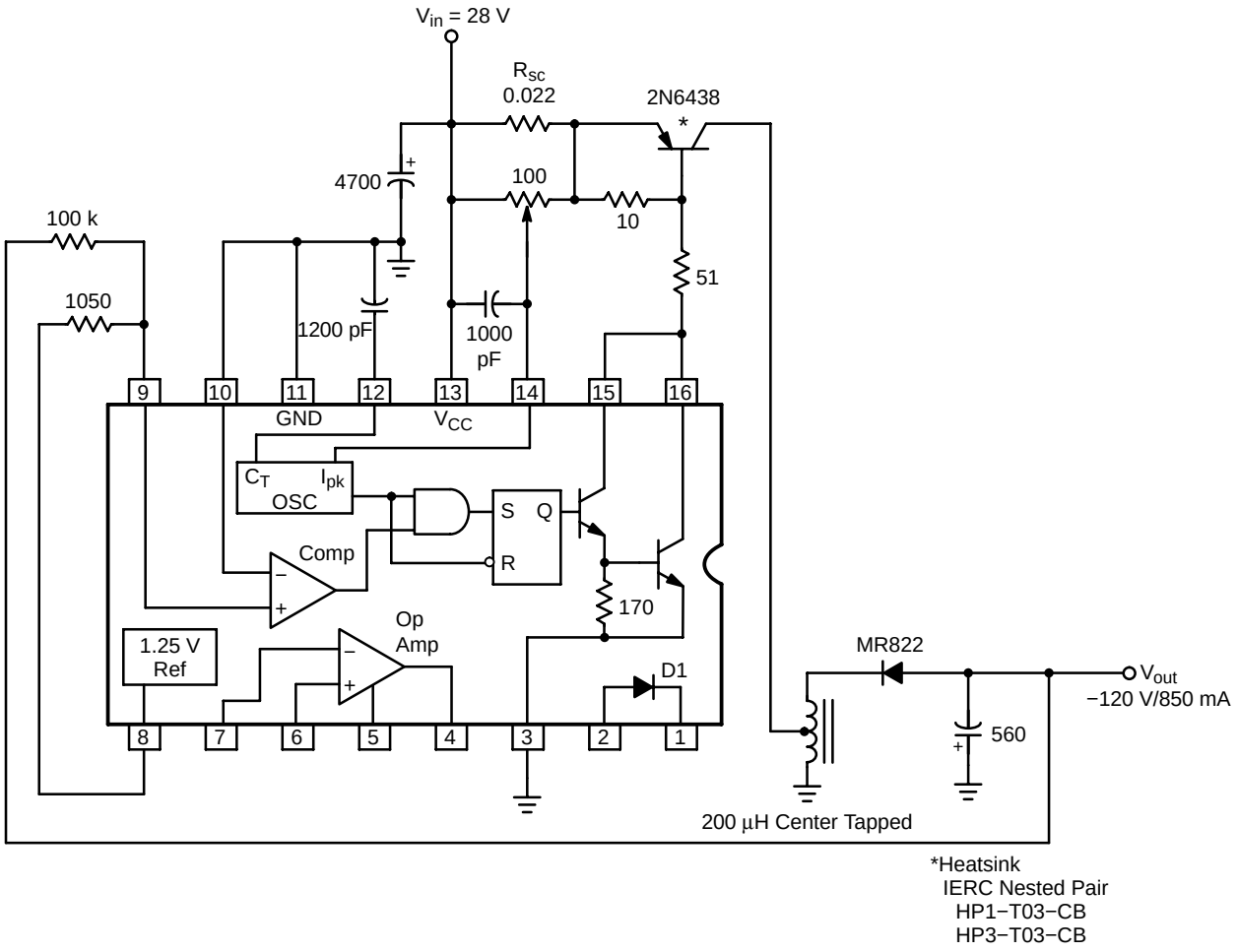
Figure 32. Dual Switcher, Step−Up and Step−Down with Buffered Switch



Test	Conditions	Results
Line Regulation	V_{in} = 4.5 to 5.0 V, I_{out} = 100 mA	Δ = 2.0 mV or ± 0.008%
Load Regulation	V_{in} = 5.0 V, I_{out} = 10 to 100 mA	Δ = 10 mV or ± 0.042%
Output Ripple	V_{in} = 5.0 V, I_{out} = 100 mA	35 mV_{p-p}
Short Circuit Current	V_{in} = 5.0 V, R_L = 0.1 Ω	1.4 A
Efficiency	V_{in} = 5.0 V, I_{out} = 100 mA	60%

The above circuit shows a method of using the MC34063 to construct a low power voltage−inverting converter. Note that the integrated circuit ground, pin 4, is connected directly to the negative output, thus allowing the internally connected comparator and reference to function properly for output voltage control. With this configuration, the sum of V_{in} + V_{out} + V_F must not exceed 40 V. The conversion efficiency is modest since the output switch is connected as a Darlington and its on−voltage is a large portion of the minimum operating input voltage. A 12% improvement can be realized with the addition of an external PNP saturated switch when connected in a similar manner to that shown in Figure 15.

Figure 33. Low Power Voltage−Inverting



Test	Conditions	Results
Line Regulation	V_{in} = 24 to 28 V, I_{out} = 850 mA	Δ = 100 mV or ± 0.042%
Load Regulation	V_{in} = 28 V, I_{out} = 100 to 850 mA	Δ = 70 mV or ± 0.029%
Output Ripple	V_{in} = 28 V, I_{out} = 850 mA	450 mV_{p-p}
Short Circuit Current	V_{in} = 28 V, R_L = 0.1 Ω	6.4 A
Efficiency	V_{in} = 28 V, I_{out} = 850 mA	81.8%

This high power voltage−inverting circuit makes use of a center tapped inductor to step−up the magnitude of the output. Without the tap, the output switch transistor would need a V_{CE} breakdown greater than 148 V at the start of t_{off}; the maximum rating of this device is 120 V. All calculations are done for the typical voltage−inverting converter with an input of 28 V and an output of −120 V. The inductor value will be 50 μH or 200 μH center tapped for the value of C_T used. The 1000 pF capacitor is used to filter the spikes generated by the high switching current flowing through the wiring and R_{sc} inductance.

Figure 34. High Power Voltage−Inverting with Buffered Switch

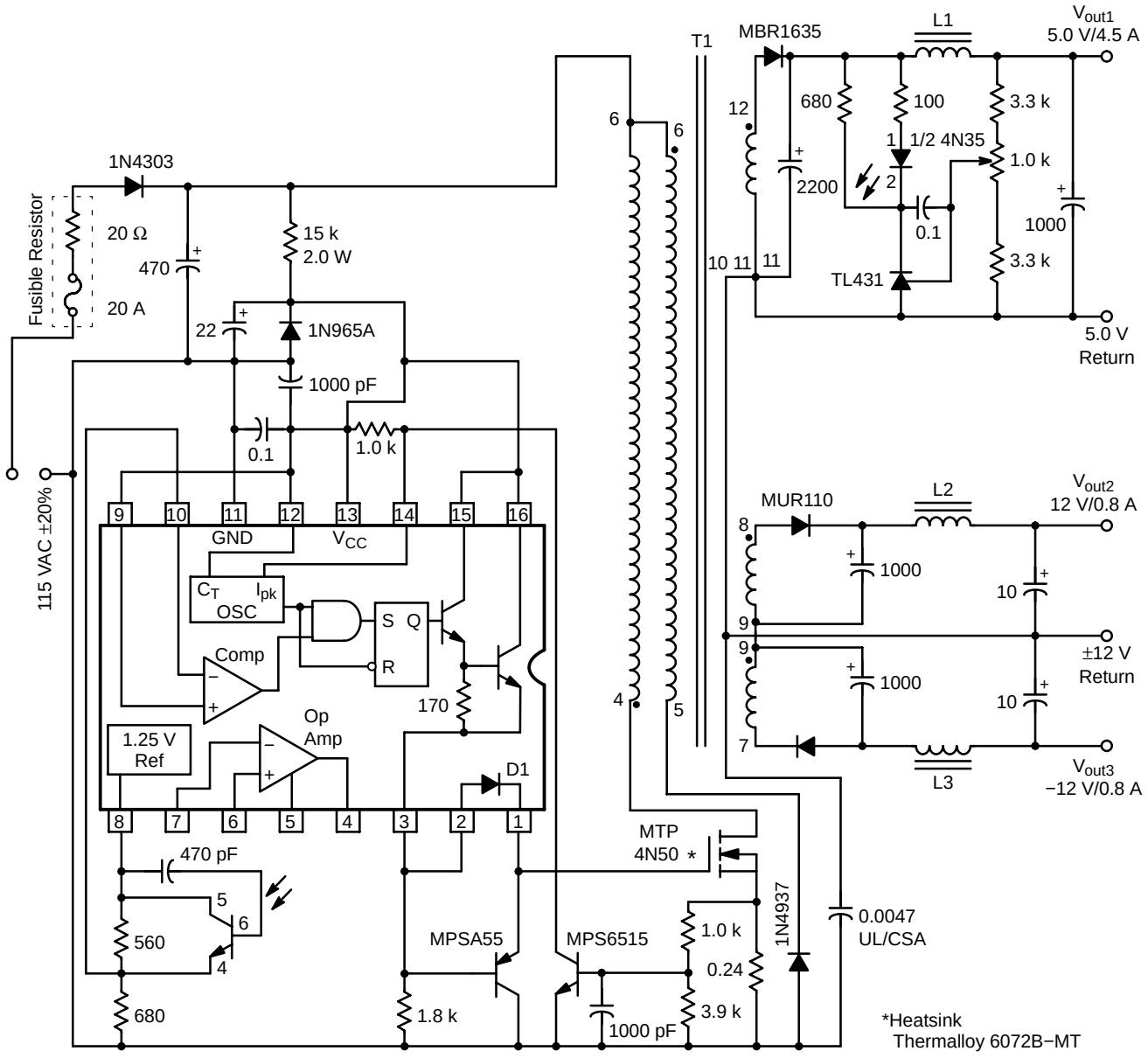
An economical 42 watt off−line flyback switcher is shown in Figure 35. In this circuit the μA78S40 is connected to operate as a fixed frequency pulse width modulator. The oscillator sawtooth waveform is connected to the noninverting input of the comparator and a preset voltage of 685 mV, derived from the reference is connected to the inverting input. The preset voltage reduces the maximum percent on−time of the output switch from a nominal of 85.7% to about 45%. The maximum must be less than 50% when an equal turns ratio of primary to clamp winding is used. Output regulation and isolation is achieved by the use of the TL431 as an output reference and comparator, and a 4N35 optocoupler. As the 5.0 V output reaches its nominal level, the TL431 will start to conduct current through the LED in the 4N35. This in turn will cause the optoreceiver transistor to turn on, raising the voltage at Pin 10 which will cause a reduction in percent on−time of the output switch.

The peak drain current at 42 W output is 2.0 A. As the output loading is increased, the MPS6515 will activate the $I_{pk(sense)}$ pin and shorten t_{on} on a cycle−by−cycle basis. If an

output is shorted, the $I_{pk(sense)}$ circuit will cause C_T to charge beyond the upper oscillator trip point and the oscillator frequency will decrease. This action will result in a lower average power dissipation for the output switching transistor.

Each output has a series inductor and a second shunt filter capacitor forming a Pi filter. This is used to reduce the level of high frequency ripple and spikes. Care must be taken with the layout of grounds in the Pi filter network. Each input and output filter capacitor must have separate ground returns to the transformer as shown on the circuit diagram. A complete printed circuit board with component layout is shown in Figure 36.

The µA78S40 may be used in any of the previously shown circuit designs as a fixed frequency pulse width modulator, however consideration must be given to the proper selection of the feedback loop elements in order to insure circuit stability.



T1 − Primary:
Pins 4 and 6 = 72 Turns #24 AWG, Bifilar Wound
Pins 5 and 6 = 72 Turns #26 AWG, Bifilar Wound
Secondary 5.0 V:
6 Turns (two strands) #18 AWG Bifilar Wound
Secondary 12 V:
14 Turns #23 AWG Bifilar Wound

T1 − Core and Bobbin: Coilcraft PT3995
Gap: 0.030″ Spacer in each leg for a primary inductance of 550 µH.
Primary to primary leakage inductance must be less than 30 µH.
L1 − Coilcraft Z7156:
Remove one layer for final inductance of 4.5 mH.
L2, L3 − Coilcraft Z7157:
25 µH at 1.0 A

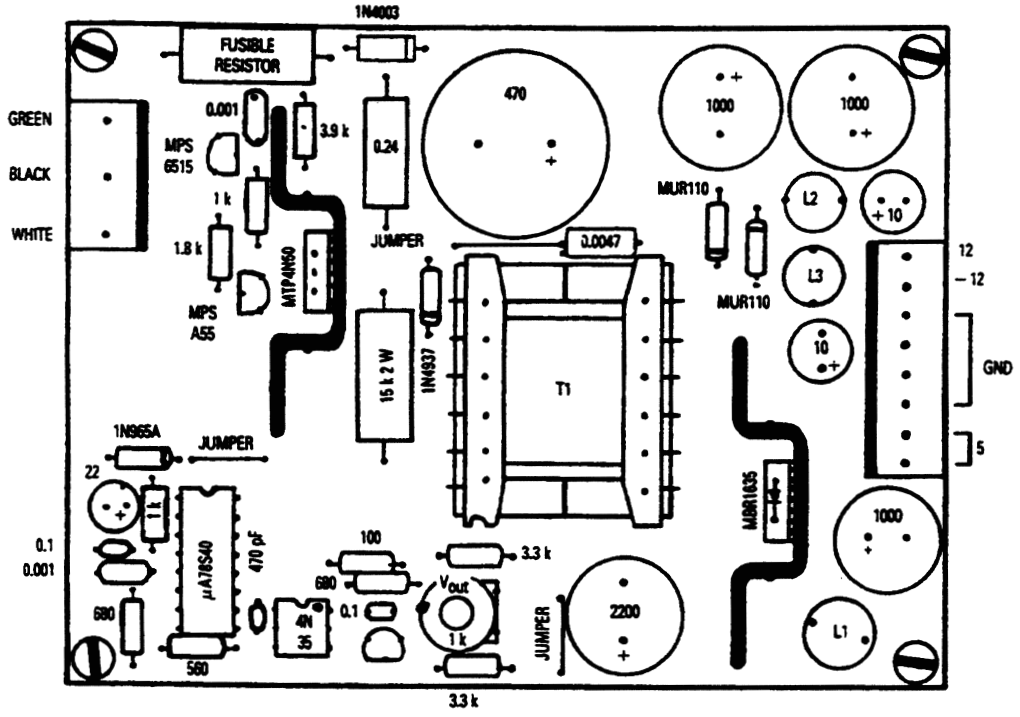
Figure 35. 42 Watt Off−Line Flyback Switcher with Primary Power Limiting

Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 92 to 138 Vac	Δ = 1.0 mV or $\pm$ 0.01%
Load Regulation	V_{out1}	V_{in} = 115 Vac, I_{out1} = 1.0 to 4.5 A	Δ = 3.0 mV or $\pm$ 0.03%
Output Ripple	V_{out1}	V_{in} = 115 Vac	40 mV_{p-p}
Short Circuit Current	V_{out1}	V_{in} = 115 Vac, R_L = 0.1 Ω	19.2 A
Line Regulation	V_{out2} or V_{out3}	V_{in} = 92 to 138 Vac	Δ = 10 mV or $\pm$ 0.04%
Load Regulation	V_{out2} or V_{out3}	V_{in} = 115 Vac, I_{out2} or I_{out3} = 0.25 to 0.8 A	Δ = 384 mV or $\pm$ 1.6%
Output Ripple	V_{out2} or V_{out3}	V_{in} = 115 Vac	80 mV_{p-p}
Short Circuit Current	V_{out2} or V_{out3}	V_{in} = 115 Vac, R_L = 0.1 Ω	10.8 A
Efficiency		V_{in} = 115 Vac	75.7%

NOTE: All outputs are at nominal load current unless otherwise noted.

Figure 35. (continued) 42 Watt Off−Line Flyback Switcher with Primary Power Limiting

Component Layout − Bottom View



Printed Circuit Board Negative − Bottom View

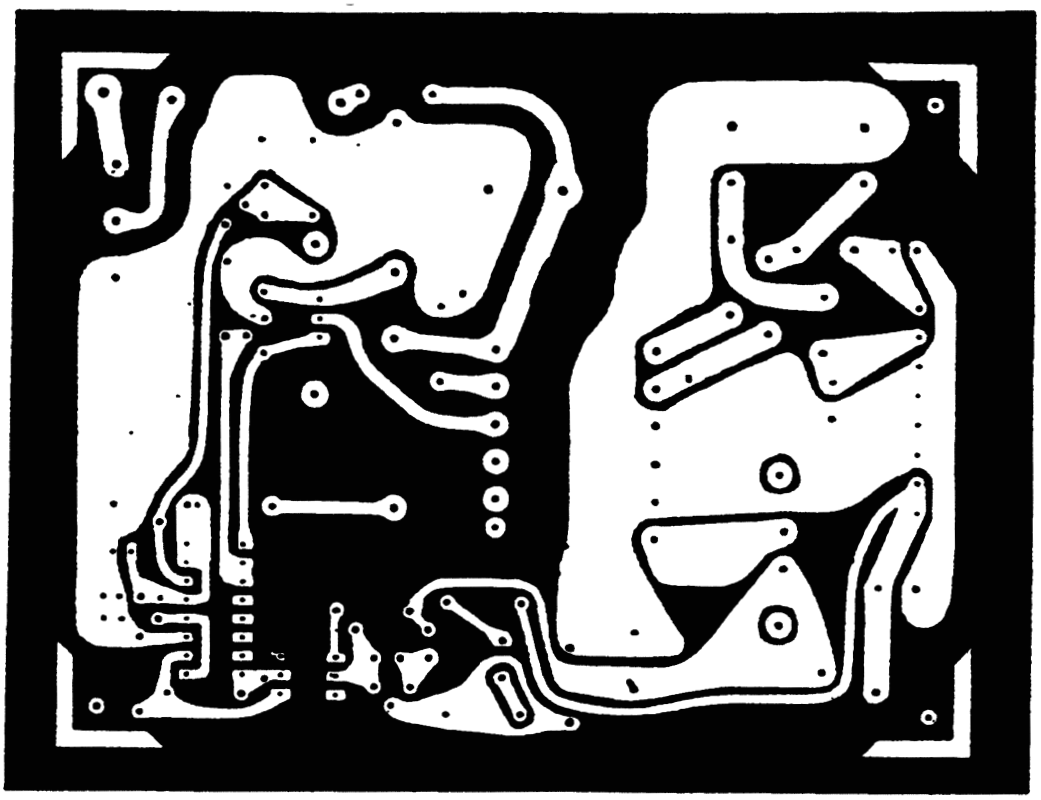
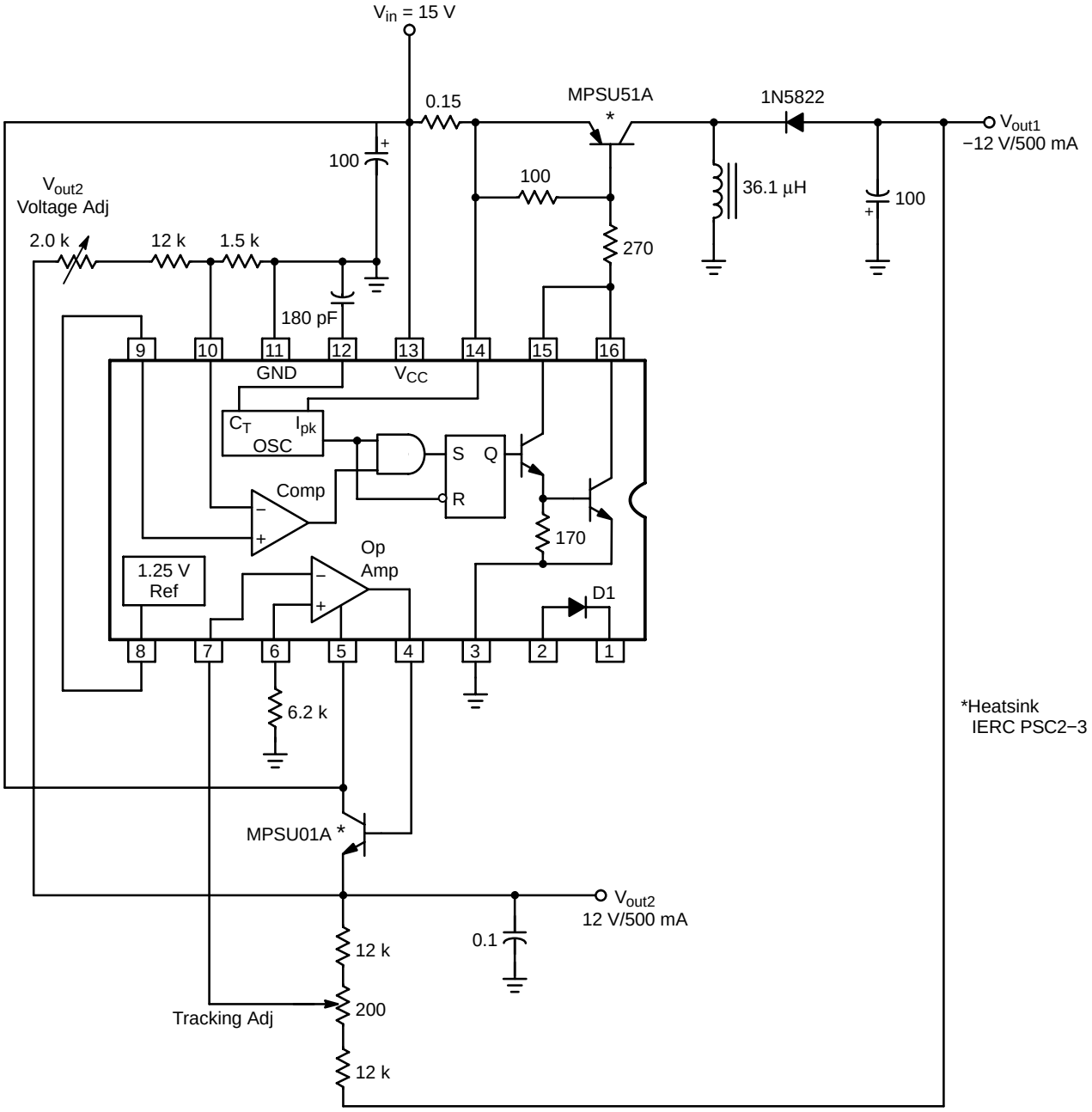


Figure 36. 42 Watt Off−Line



Test		Conditions	Results
Line Regulation	V_{out1}	V_{in} = 14.5 to 18 V, I_{out1} = 500 mA, I_{out2} = 500 mA	Δ = 10 mV or ± 0.042%
Load Regulation	V_{out1}	V_{in} = 15 V, I_{out1} = 100 to 500 mA, I_{out2} = 500 mA	Δ = 2.0 mV or ± 0.008%
Output Ripple	V_{out1}	V_{in} = 15 V, I_{out1} = 500 mA, I_{out2} = 500 mA	125 mV_{p-p}
Line Regulation	V_{out2}	V_{in} = 14.5 to 18 V, I_{out1} = 500 mA, I_{out2} = 500 mA	Δ = 10 mV or ± 0.042%
Load Regulation	V_{out2}	V_{in} = 15 V, I_{out2} = 100 to 500 mA, I_{out1} = 500 A	Δ = 5.0 mV or ± 0.021%
Output Ripple	V_{out2}	V_{in} = 15 V, I_{out1} = 500 mA, I_{out2} = 500 mA	140 mV_{p-p}
Efficiency		V_{in} = 15 V, I_{out1} = 500 mA, I_{out2} = 500 mA	77.2%

This tracking regulator provides a ±12 V output from a single 15 V input. The negative output is generated by a voltage−inverting converter while the positive is a linear pass regulator taken from the input. The ±12 V outputs are monitored by the op amp in a corrective fashion so that the voltage at the center of the divider is zero ± V_{IO}. The op amp is connected as a unity gain inverter when $|V_{out1}| = |V_{out2}|$.

Figure 37. Tracking Regulator, Voltage−Inverting with Buffered Switch and Buffered Linear Pass from Input

SUMMARY

The goal of this application note is to convey the theory of operation of the MC34063 and μA78S40, and to show the derivation of the basic first order design equations. The circuits were chosen to explore a variety of cost effective and practical solutions in designing switching converters. Another major objective is to show the ease and simplicity in designing switching converters and to remove any mystical “black magic” fears. ON Semiconductor maintains a Linear and Discrete products applications staff that is dedicated to assisting customers with any design problems or questions.

BIBLIOGRAPHY

Steve Hageman, *DC/dc Converter Powers EEPROMs*, *EDN*, January 20, 1983.

Design Manual for SMPS Power Transformers, Copyright 1982 by Pulse Engineering.

HeatSink/Dissipator Products and Thermal Management Guide, Copyright 1980 by International Electronic Research Corporation.

Linear and Interface Integrated Circuits Data Manual, Copyright 1988 by Motorola Inc.

Linear Ferrite Materials and Components Sixth Edition, by Ferroxcube Corporation.

Linear/Switchmode Voltage Regulator Hanbook Theory and Practice, Copyright 1989 by Motorola Inc.

Molypermalloy Powder Cores, Catalog MPP−303U, Copyright 1981 by Magnetics Inc.

Motorola Power Data Book, Copyright 1989 by Motorola Inc.

Motorola Rectifiers and Zener Diodes Data Book, Copyright 1988 by Motorola Inc.

Structured Design of Switching Power Magnetics, *AN−P100*, by Coilcraft Inc.

Switching and Linear Power Supply, Power Converter Design, by Abraham I. Pressman, Copyright 1977 by Hayden Book Company Inc.

μA78S40 Switching Voltage Regulator, Application Note 370, Copyright 1982 by Fairchild Camera and Instruments Corporation.

Switchmode Transformer Ferrite E−Core Packages, *DS−P200*, by Coilcraft Inc.

Jim Lange, *Tapped Inductor Improves Efficiency for Switching Regulator, ED 16*, August 2, 1979.

Voltage Regulator Handbook, Copyright 1978 by Fairchild Camera and Instruments Corporation.

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Mallory Capacitor Co.
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