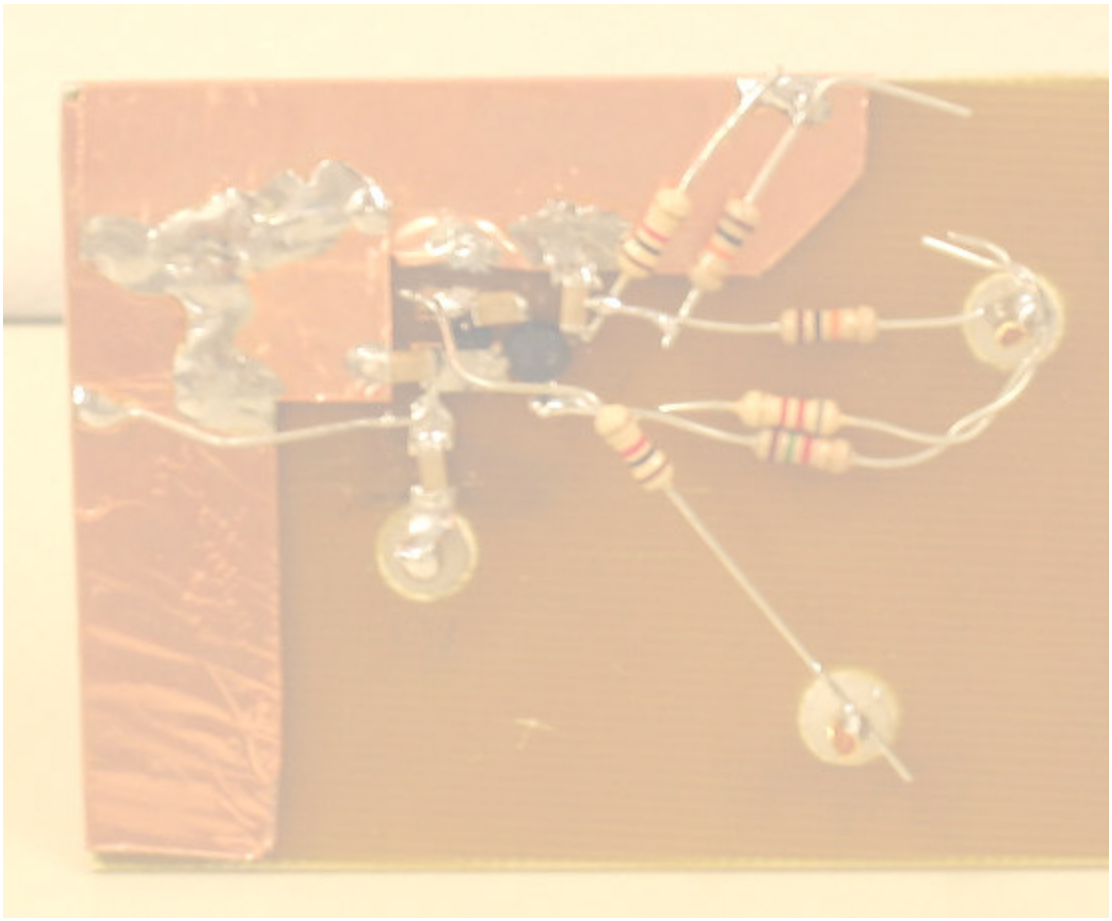
EE414: RF Transceiver Design Lab

Stanford University

Professor: Thomas Lee



Lab Exercise 4: Phase-Locked VCO Design

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1. Introduction

The purpose of this laboratory is to design, build and test a crystal locked voltage controlled oscillator (VCO). The specifications are listed below:

Table 1. Design specifications

Parameter	Specification	Notes
VCO Tuning Frequency	<900MHz to >1GHz	PLL control range 0.5V to 5V
Output Power	>0dBm	Can be as high as 7dBm
Reference Spur	<-30dBc	
Phase noise		As low as possible
Phase Margin	>45°	

An overall block diagram of a crystal driven phase-locked VCO is shown in Figure 1. The blocks in the blue background are all integrated in the Motorola MC12181 synthesizer chip. A 25MHz crystal was used to drive the synthesizer chip and a loop filter and VCO were designed as part of this laboratory exercise.

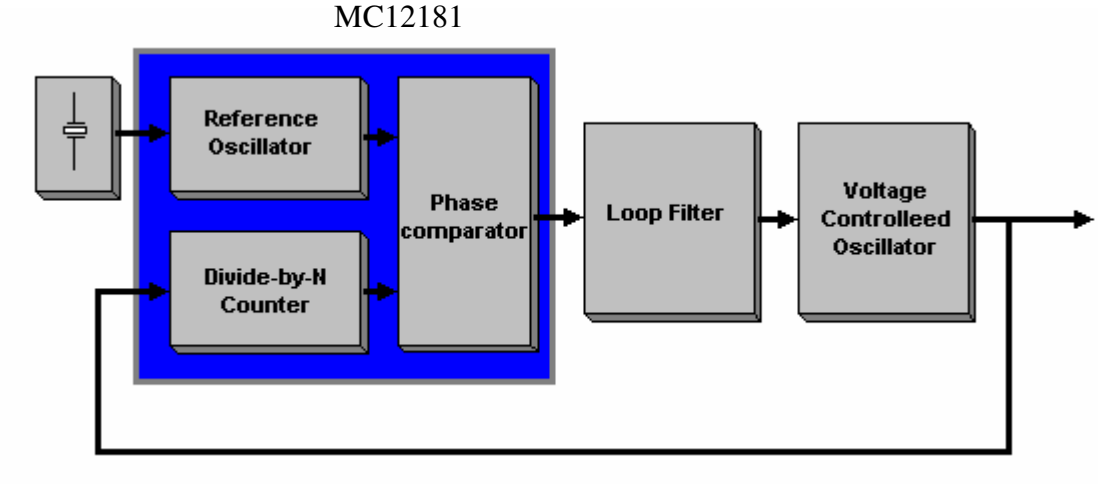

Figure 1: Block diagram of PLL VCO

2. VCO Design

We chose a basic Colpitts (Figure 2) topology for the VCO. A microstrip line serves as the tank inductance. The VCO was designed to oscillate at 1GHz. However due to the unwanted lead inductance of the varactor and additional parasitic inductance, we were unable to get the VCO to oscillate above 800MHz. Repeated building of the board with varactors in parallel and all key

capacitors in parallel provided only negligible increase in frequency. Nominal oscillations with this basic topology were around 700MHz within the 0.5V to 5V tuning range. We remain unconvinced that this topology can indeed yield 1GHz oscillations without some additional techniques such as level shifting.

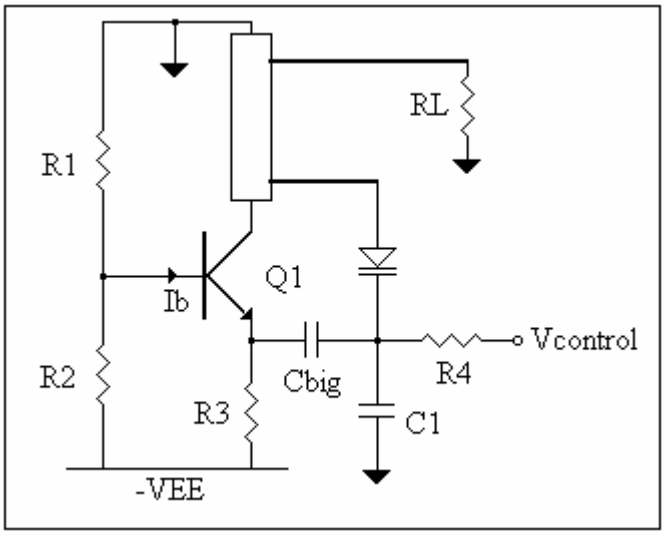

Figure 2: Basic Colpitts topology.

To raise the oscillation frequency to about 1GHz, either the equivalent tank inductance or capacitance has to be reduced. Adjusting the length of the microstrip inductor to almost zero had negligible impact on the oscillation frequency. In fact it can be shown[1] that any series inductance with the varactor adds directly to the overall inductance of the tank, and therefore serves to reduce the expected oscillation frequency.

By trial and error we discovered that removing C1 altogether, yielded good performance with oscillations that tuned within the specified range with sufficient output power and stable spectrum. By using C_Π of the BJT as our shunt capacitance in series with the varactor, we recognized we had two knobs to tune and optimize the circuit behavior. One knob was the varactor voltage and another knob was the BJT bias current which controls the value of C_Π. After much optimization, we realized we needed an 9V to 14V range for the varactor control voltage. This control voltage range yields varactor capacitances small enough to dominate the overall tank capacitance and result in a wide tuning range.

[1] Deji Akinwande has shown this in a document explaining this effect to the EE414 class. This document is available on the EE414 Spring 2005 webpage (http://eeclass.stanford.edu/cgi-bin/announcements.cgi?cc=ee414)

We implemented a single-supply non-inverting op-amp to level shift and amplify the PLL control range to our desired varactor bias range. The op-amp gain is 3. The final schematic and values are shown in Figure 3. Figure 4 is a picture of the actual VCO board.

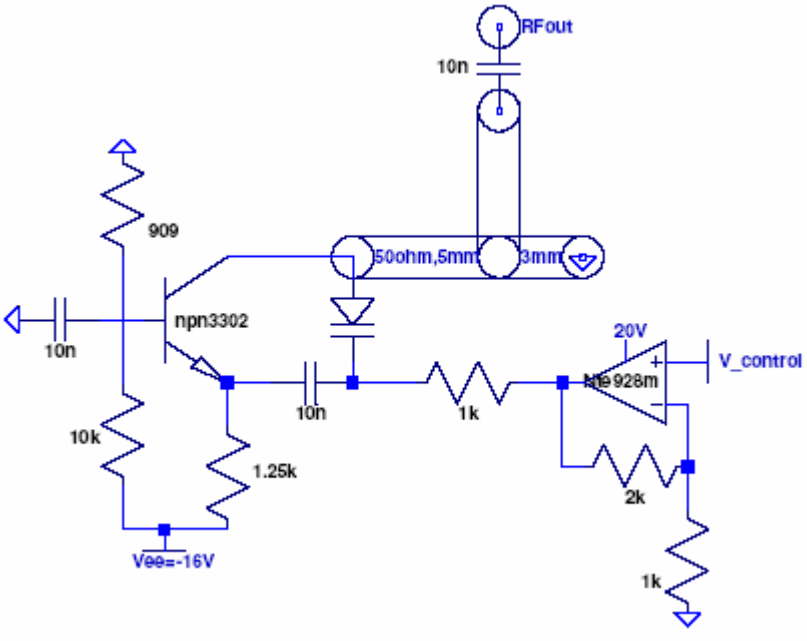

Figure 3: Equivalent Schematic of the VCO and op-amp level shifter with component values

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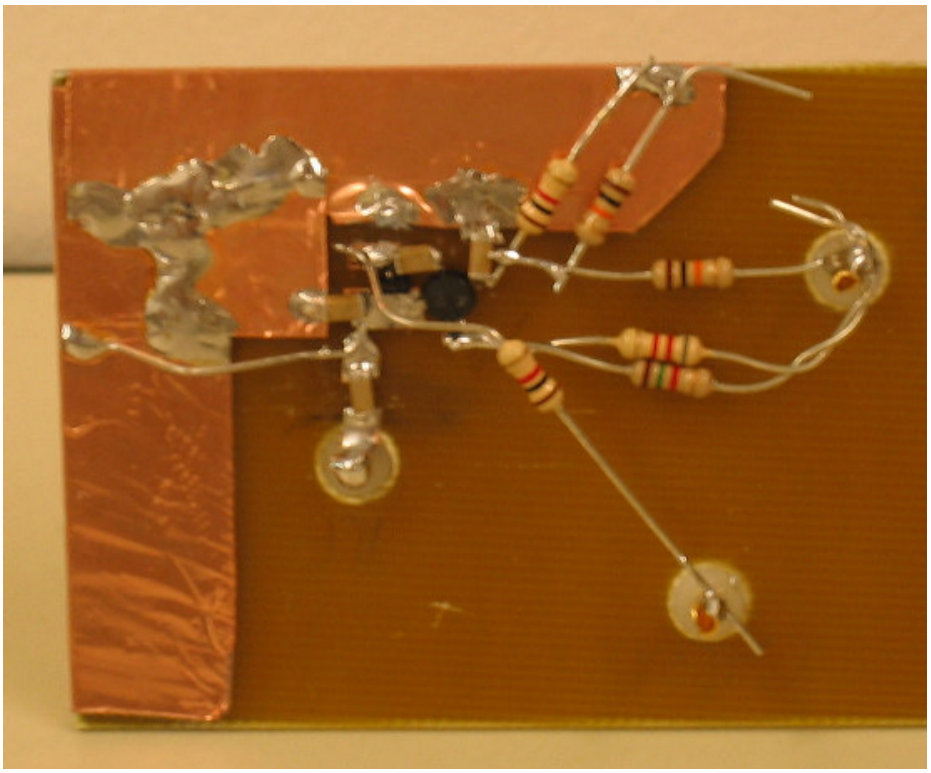


Figure 4: Picture of VCO board.

2.1 VCO Tuning Range and Linearity

Much effort was spent on obtaining a monotonically increasing oscillation frequency with voltage characteristics. On one of our boards (14dBm 1GHz output) we observed at least one discrete jump in frequency around 925MHz. This jump was most likely due to radiative coupling influence on our control voltage. Local shielding of the RF signal transmission line did not provide repeatable improvements. Our final board (shown in Figure 4) was a few dB less in output power with better isolation of the signal line from the control line in the board layout.

The frequency vs. control voltage profile is shown in Figure 5. The VCO tunes from 675MHz to 1020MHz with a control voltage of 1V to 5V. A control voltage of about 2.7V yields an oscillation of 900MHz. The slope is fairly monotonic and generally well-behaved. The average slope value is about 50MHz/V with the actual slope varying from about 40MHz/V to 60MH/V. The saturation of frequency at high control voltage is due to the saturation of the varactor capacitance. For example, due to the multiplication from the non-inverting op-amp, the actual varactor reverse voltage is 15V at a control input of 5V. At 15V, the varactor capacitance has begun to saturate.

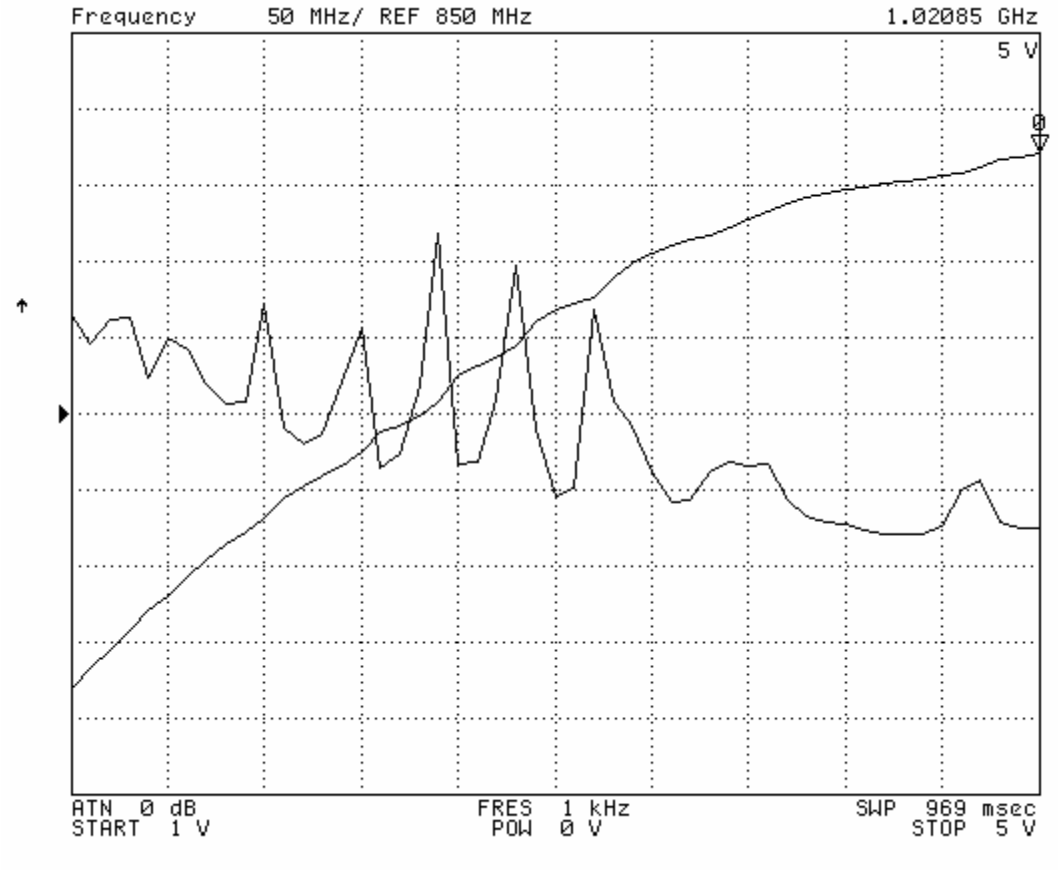


Figure 5: VCO frequency vs. Control Voltage response. The jagged curve is the phase noise analyzer estimate of the local slope in MHz/V.

2.2 VCO Output Power

The oscillation output power vs. control voltage is shown in Figure 6. The minimum output power in the specified band is 3dBm at 900MHz. The power at 1GHz is 7dBm. These range of powers falls nicely within the specified output power range. The output power increases with frequency due to the decreasing capacitive turns ratio (n_c) and resulting increase in resonant tank voltage as control voltage increases. The increase in power can be shown in the equation below:

$$V_{\tan k} = 2I_{Bias}R_{\tan k} \text{ ,where } R_{\tan k} \approx \left(\frac{50}{n_L^2}\right) \| \left(\frac{1}{n_C^2 G_m}\right), \text{ and } n_C = \frac{C_{\text{var}\,actor}(V)}{C_{\text{var}\,actor}(V) + C\pi} \quad (1)$$

where n_L is the inductive turns ratio and G_m is the large signal transconductance. The factor of 50 is the load resistance. The approximate sign results from the neglect of an emitter bias resistor and the finite Q of FR4 microstrip lines.

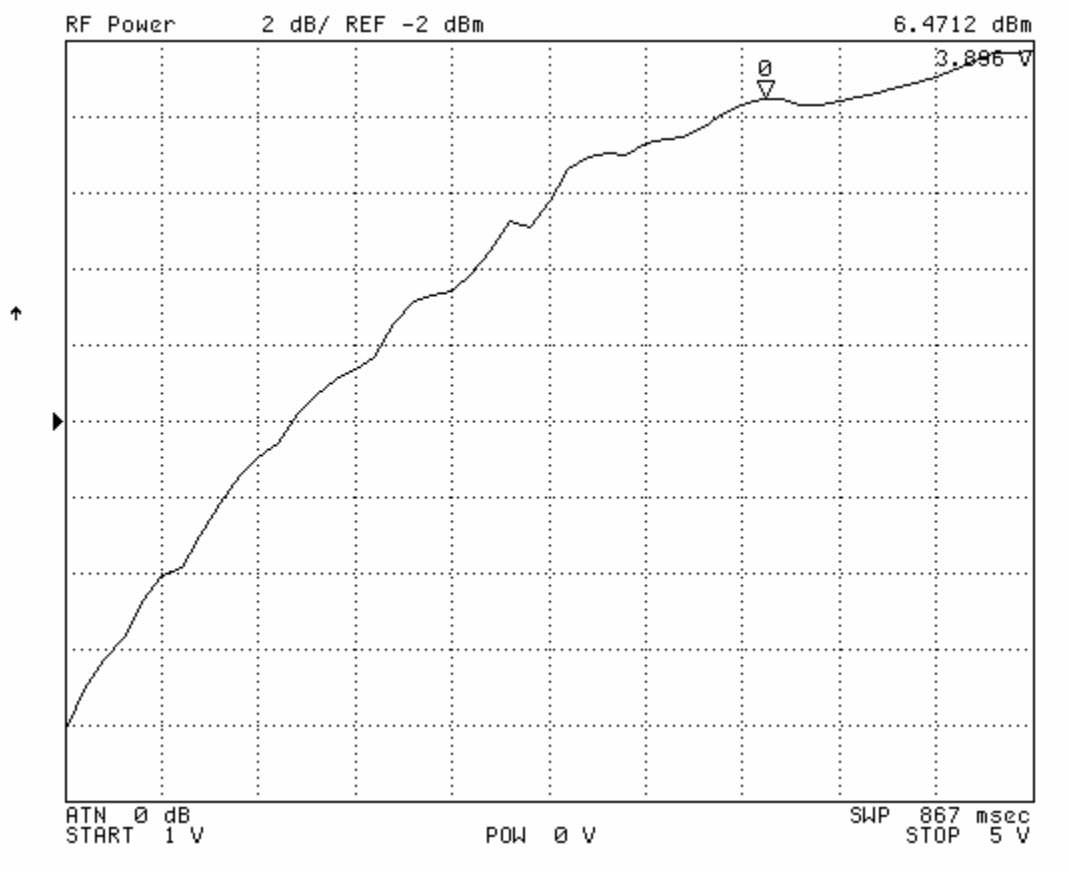


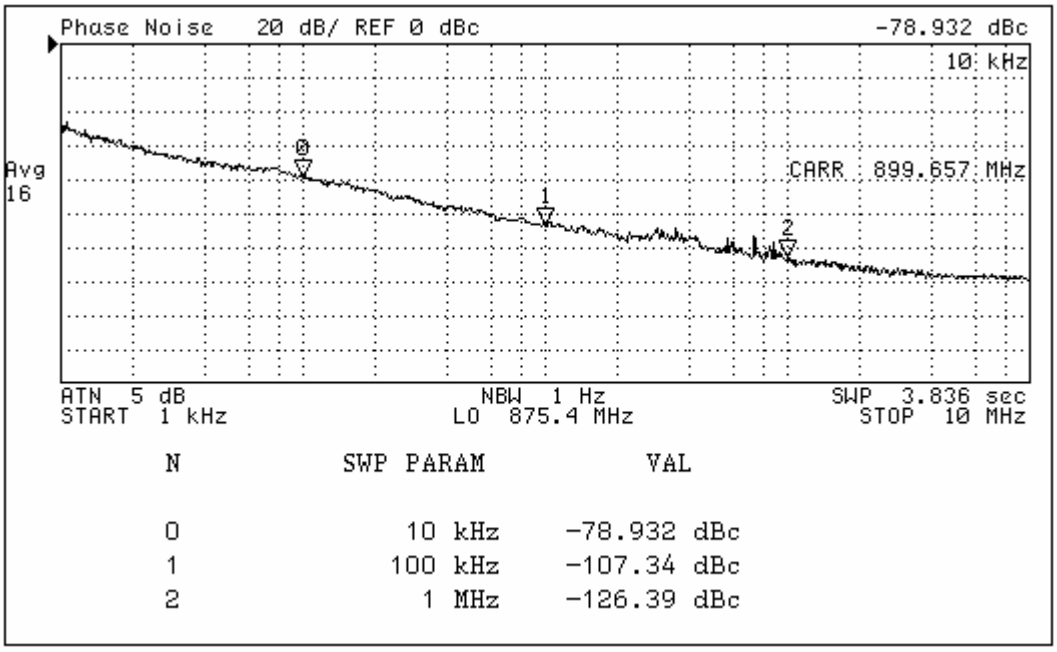
Figure 6: VCO Output Power vs. Control Voltage profile. The power is 7dBm at 1GHz and 3dBm at 900MHz.

2.3 VCO Phase Noise and Overall Performance

The phase noise of the VCO was measured at 900MHz, and 1GHz. The noise profiles follow the expected initial quasi-linear profile and eventual noise saturation of textbook VCOs. This profile 'roughly' results from the device and circuit noise originally centered at DC been transferred and re-centered around the oscillation frequency. The measured close-in and far out phase noise are recorded in the plots shown in Figure 7. The overall performance of the VCO with op-amp level shifter is reported in Table 2.

Table 2: VCO (with level-shifter) summary

Frequency	**900 MHz**	**1 GHz**
Bias Voltage	2.7 V	4.4 V
Power	3 dBm	7 dBm
Phase noise @ 10 kHz	-78.9 dBc	-89.5 dBc
Phase noise @ 100 kHz	-107.3 dBc	-117.4 dBc
Phase noise @ 1 MHz	-126.4 dBc	-137.6 dBc



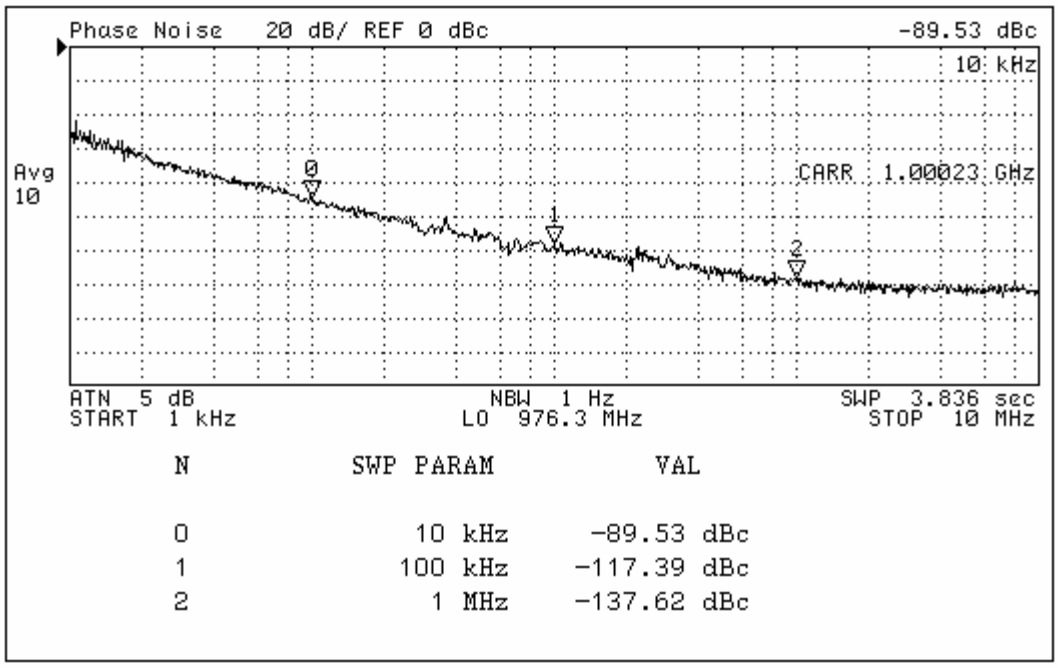


Figure 7: Phase noise profile of the VCO.

3.0 Linearized PLL Model

The purpose of a PLL is to confer the phase stability of a crystal oscillator to a VCO, with the assumption that the crystal oscillator has superior phase noise at least within the bandwidth of the phase lock loop. Essentially the PLL is a non-linear feedback, but after lock has been achieved, it can be described in linear terms with regards to phase. The input phase perturbations are transferred to the output by a linear transfer function. At an elementary level, the linearized loop can be thought of as a band-limited ideal op-amp. The differential inputs of the op-amp are driven by Φin and Φout, and the op-amp output is Φout. Due to the infinite gain of the op-amp, it forces Φout to be identical to Φin. Essentially, the linearized PLL model is an op-amp operating as a follower.

A linearized model of the specific PLL for this lab is shown in Figure 8. In the model, Φe is the phase error which is converted to current (Ip) by the charge pump, and then passes through a low-pass filter. The resulting control voltage subsequently drives the VCO.

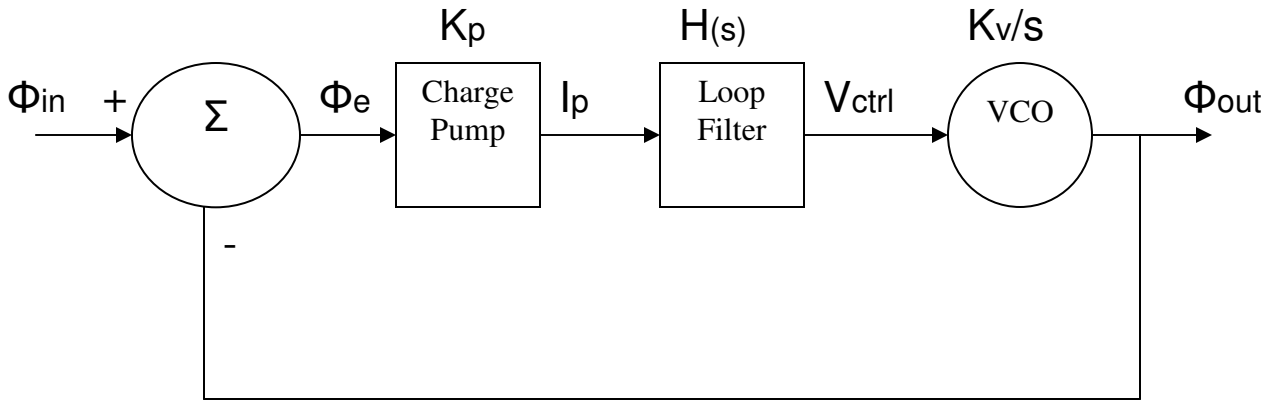


Figure 8: A linearized PLL model.

The charge pump is modeled as a constant transfer function Kp, while the VCO is modeled as a single pole transfer function. The loop filter for this lab is a 3rd-order loop filter and is described in the next section. The filter's transfer function for the filter shown in Figure 9 is:

$$H(s) = K_F \frac{1 + sRoCo}{s[1 + sRo(Co \| Ca)][1 + sCx(\mathrm{Re}q + Rx)]} \tag{2}$$

where $\mathrm{Re}q = K_F \frac{1 + sRoCo}{s[1 + sRo(Co \| Ca)]}$, and $K_F = \frac{1}{Co + Ca}$ (3)

For this lab, Req is negligible compared to Rx and can be ignored for all frequencies of interest. The transfer function for a charge pump is simply Kp=Ip/2Π. The closed loop transfer function relating the output phase to the input phase is

$$\frac{\Phi_{out}}{\Phi_{in}} = G(s) = \frac{1}{1 + \frac{s}{K_P H(s) K_V}} \tag{4}$$

Without any complicated analysis, a visual inspection of G(s) reveals that the output phase matches the input phase up to a certain bandwidth called the loop bandwidth. Herein lies the magic of the PLL, it transfers the phase stability of a superior crystal oscillator to a VCO.

3.1 PLL Loop Filter Design

The loop filter was designed using Hamid Rategh's recipe. As suggested in the synthesizer's datasheet, a 3rd-order filter was designed resulting in a 4th-order PLL. A 3rd-order loop filter

provides more attenuation of out-of-band ripples resulting in a cleaner spectrum. However, due to the additional poles in the filter, the PLL can potentially become unstable. Some stability is provided by the zero formed by Ro and Co. The behavior of the loop filter can be explained as follows: Ro, Co forms a zero which is ideally located between a DC pole and two higher frequency poles (see equation (2)).

Stability was the primary emphasis in the loop filter design due to the presence of an additional pole from the op-amp and the uncertainty of the location of the op-amp's pole[2]. We designed the loop filter for a lower cross-over than that suggested (100KHz) in the lab handout and a higher phase margin. Our initial calculations were for a target cross-over frequency of 50KHz, and a phase margin of 60°. After rounding the calculated values to the values available in the lab, our final cross-over frequency is about 50KHz with a phase margin of about 55°. The final values are shown in Figure 9 and the magnitude and phase response of the loop filter in Figure 10.

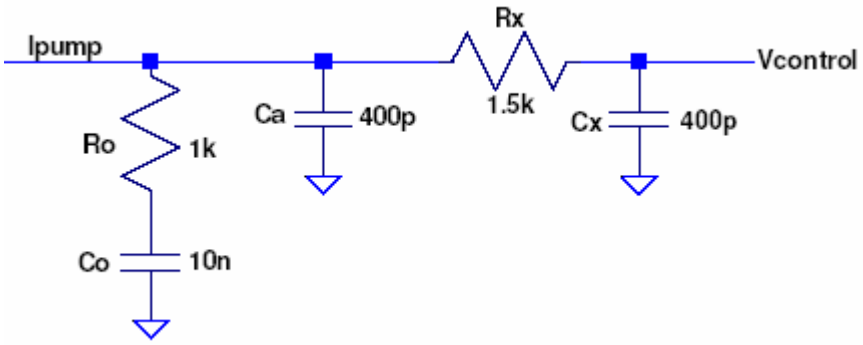


Figure 9: Loop Filter schematic with final values.

[2] The NTE928M single supply Op-Amp's datasheet provides no frequency response information whatsoever.

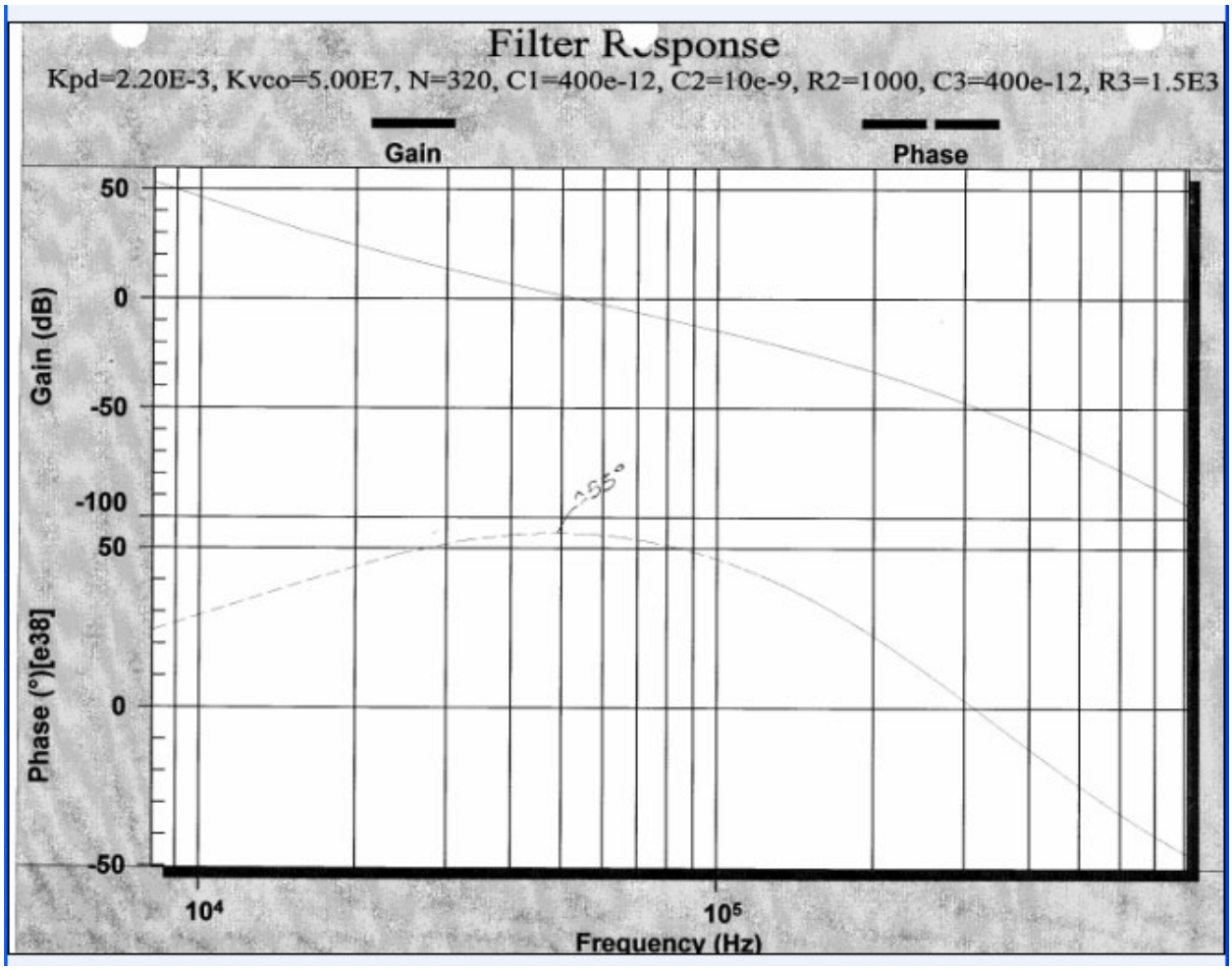


Figure 10: Magnitude and Phase response plotted using National Semiconductor loop filter program. The cross-over occurs at 50KHz with phase margin of about 55°.

3.2 PLL and VCO Integration

The synthesizer, crystal, crystal capacitors and bypass capacitors were all mounted on a ready made printed circuit board (PCB). Additionally, the loop filter and the op-amp level shifter were also mounted on the PCB. The crystal was verified to operate at a fundamental tone of 25MHz by mounting it on a microstrip board and measuring the first resonant frequency. A picture of the PLL board is shown in Figure 11.

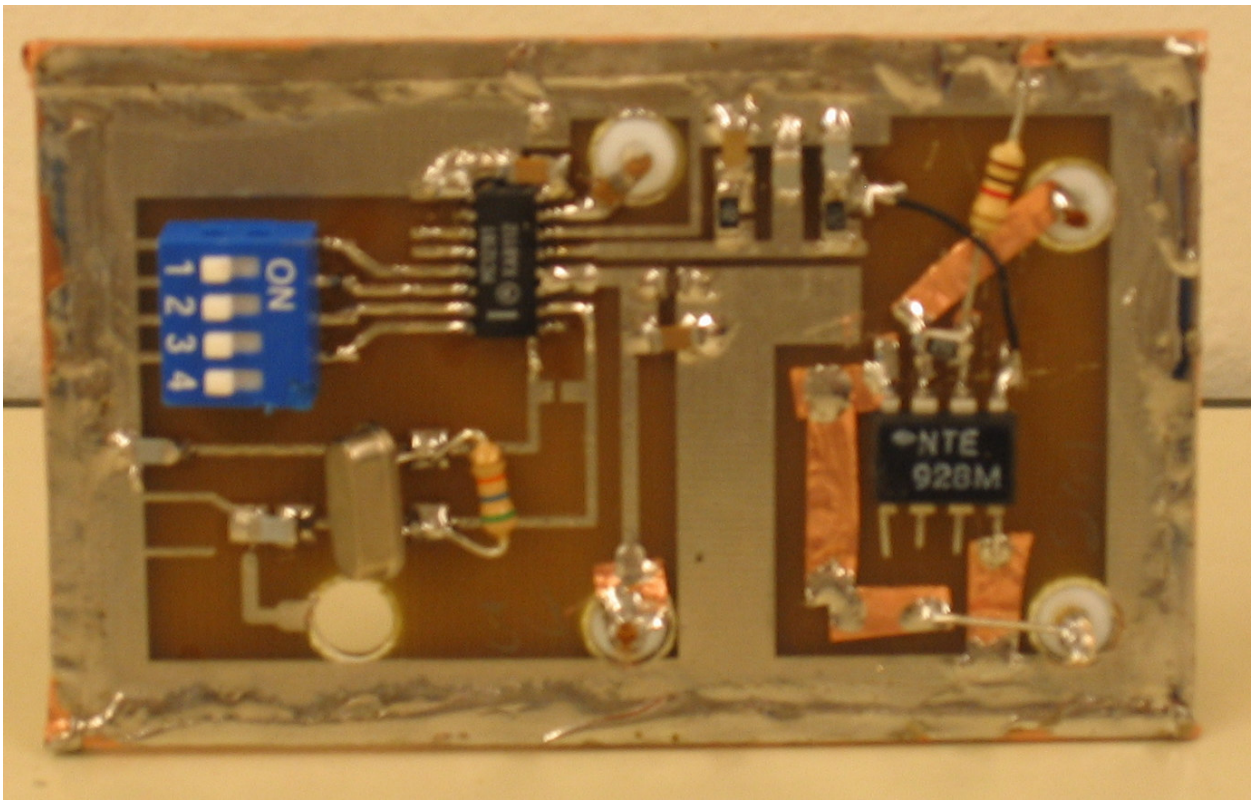


Figure 11: Picture of the PLL board with synthesizer, crystal, loop filter and op-amp level shifter.

3.3 Phase-Locked Output Signal and Phase noise

The PLL was connected to drive the VCO, and surprisingly they worked together to our great relief[3]. The PLL locked the VCO at 1GHz and 975MHz. The spectrum of a 1GHz output as measured with the spectrum analyzer is shown in Figure 12. The reference spurs are clearly visible and are about 60dBc down. These reference spurs arise from the leak-out of the undesired fundamental harmonic that is produced in the phase comparison process which is at a rate of 3.125MHz. Fortunately, the spurs are very low due to the strong rejection of the loop filter. The oscillation output power is about 0dBm. A later tweak to the board increased the power to about 2dBm. We expect this will be sufficient to drive a mixer stage.

[3] Actually, the reported PLL was our 2nd (backup) board. Our 1st board (14dBm output) proved to wild to be tamed by the PLL.

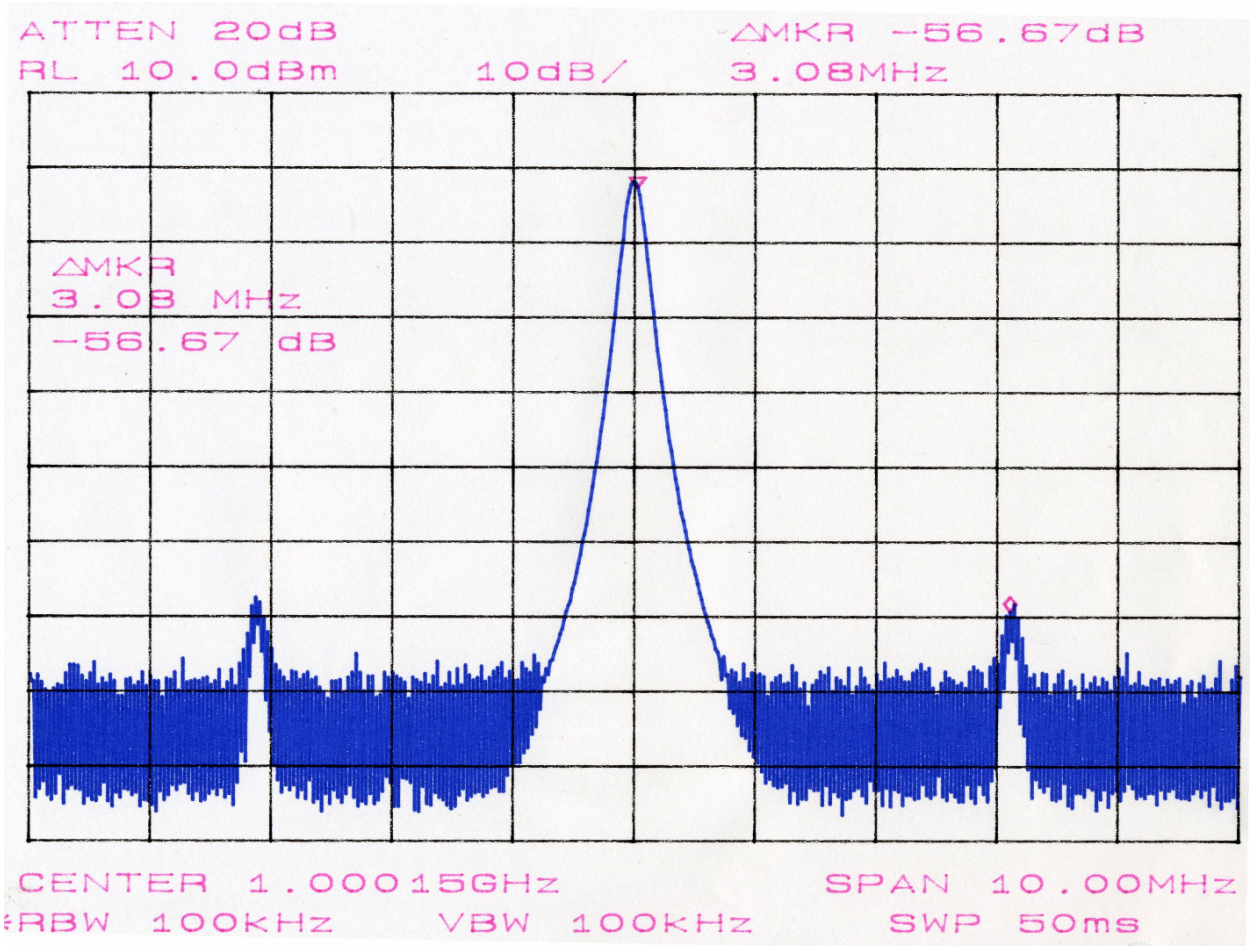


Figure 12: Spectrum of phase-locked 1GHz output with 3.1MHz (60dBc) reference spurs.

The phase noise is shown in Figure 13. The close-in phase noise is as low as 80dBc/Hz due to the superior phase stability of the crystal. The crystal's phase blessings on the VCO extend to about 10KHz and a transition occurs to the inherent VCO phase noise. The 10KHz bandwidth is very close to our loop bandwidth target.

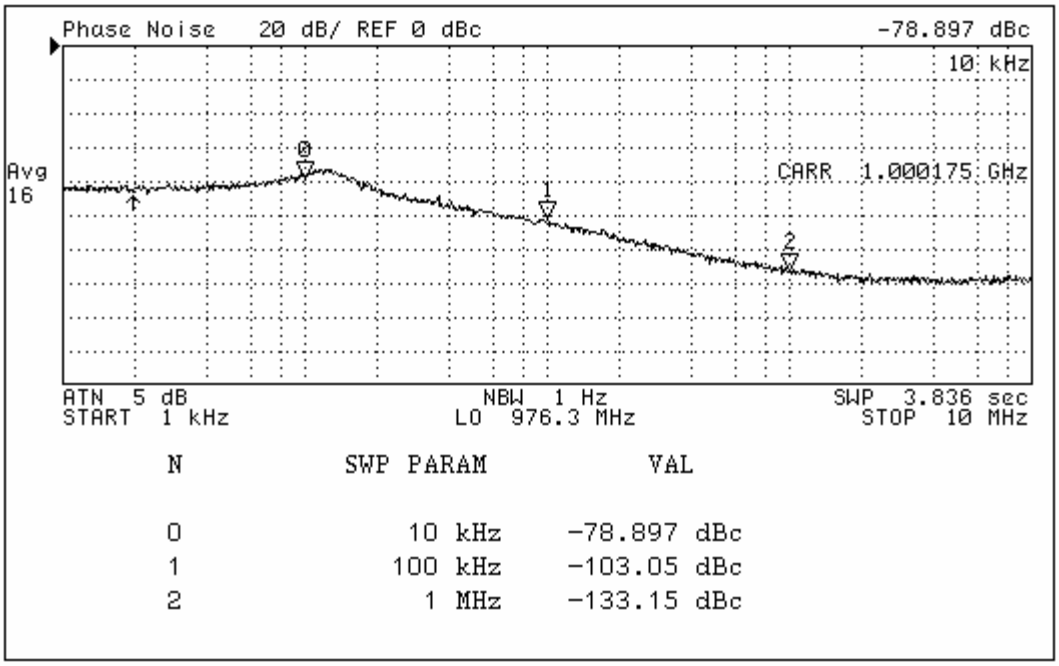


Figure 13: Phase noise of a 1GHz phase-locked VCO.

4.0 Conclusion

The overall effect of the PLL on the VCO is to improve the close-in phase noise (or stability), and reduce the VCO output power (due to feedback sampling). After endless days and seemingly endless nights, we report the goodness of an improved phase noise with enough power left to drive a mixer stage. A comparison of the open-loop VCO and the phase-locked VCO at 1GHz is shown in Table 3. A clear 30dB improvement in phase noise is seen at 1KHz. At 1MHz offset, the PLL/VCO phase noise approaches that of the open-loop VCO.

Table3: Open-loop VCO and closed-loop VCO comparison at 1GHz

Frequency	**Open-loop VCO**	**Closed-loop VCO**
Power	7 dBm	2 dBm
Phase noise @ 1 kHz	-50 dBc	-81 dBc
Phase noise @ 10 kHz	-89.5 dBc	-78.9 dBc
Phase noise @ 100 kHz	-117.4 dBc	-103 dBc
Phase noise @ 1 MHz	-137.6 dBc	-133 dBc

This lab has been more than a learning experience. It has been an adventure in team and group work, team stress, frustration and emotional panic depression. We take pleasure in our success and declare victory in accomplishing this lab. We look forward to integrating everything together for the transceiver operation.