OCTAVE TUNING, HIGH FREQUENCY VARACTOR OSCILLATOR DESIGN

by

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Octave Tuning, High Frequency Varactor Oscillator Design

Thesis directed by Professor Zoya Popović

Octave tuning varactor oscillators have been used with great success in sub-3GHz microwave systems and measurement equipment. This work focuses on extending the state of the art in both frequency range and phase noise performance. A 1.9Ghz to 3.8GHz octave tuning varactor oscillator and related design are presented. The oscillator demonstrated a measured phase noise of -105dBc at 100kHz offset at 3.8GHz with an output power of 3dBm. Performance enhancements are discussed as well as theoretical limitations.

DEDICATION

I dedicate this work to my parents for their love, support and understanding. I also dedicate this to my girlfriend, Cindy, for her love, patience and compassion she has shown me during our time apart and together. And to Emma, may I never be without a frisbee.

ACKNOWLEDGEMENTS

This work was made possible by a fellowship from Agilent Technologies. I thank Jerry Gladstone for all his efforts to make this happen. I also thank Dan Harkins and Dean Nicholson for supporting my graduate degree and allowing me to take 9 months off from work. Stefania Römisch has provided a wealth of information and understanding. Her lively discussions gave valuable insight to many of the problems brought up throughout the year. I thank Zoya Popović for being my graduate advisor and her wonderful guidance.

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CHAPTER 1

INTRODUCTION

1.1 Introduction to Oscillators

Oscillators are fundamental building blocks of any communication or test and measurement system. They are used in virtually all upconversion, downconversion, frequency modulation and high frequency generation systems. While most oscillators are designed to generate a sinusoidal voltage waveform, the uses and required performance varies widely.

An important distinction in oscillators stems from their frequency tunability. Fixed frequency oscillators are generally very stable and optimized for heterodyne upconversion and downconversion systems in satellite communication and GPS navigation. A fixed frequency oscillator exhibits excellent short term stability and very low long term drift.

Tunable oscillators may in turn be separated into two groups, narrowband and wideband. A narrowband oscillator may have a tunable range between 5% and 10% and is commonly used in communication systems that require small amounts of tuning such as channel selection in cellular phones.

Wideband oscillators are able to tune over an octave and some up to a decade of frequencies. They are used in systems requiring broad frequency range tunability such as radar systems, highly adaptive communication systems and measurement equipment. The use of wideband oscillators in measurement equipment will be the focus of the work presented here.

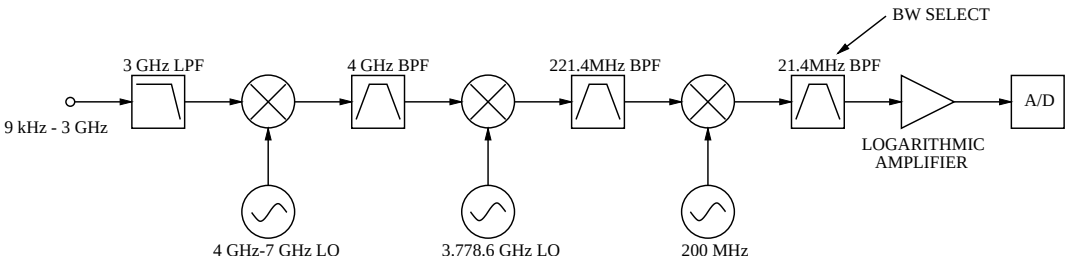


Figure 1.1. Block diagram of a spectrum analyzer using triple heterodyne downconversion.

1.2 Oscillators in Test and Measurement Equipment

Wideband oscillators are used in spectrum analyzers, frequency sweepers and network analyzers. Frequency domain test and measurement systems pose interesting challenges for oscillator design. The test system must be versatile enough to work over a broad range of frequencies, meet or exceed the performance of the device under test (DUT) and must not alter the function or performance of the DUT.

A spectrum analyzer is a good illustrator of these design criteria. The function of a spectrum analyzer is to sample a very small bandwidth (BW) of frequency and display the amount of power contained in it. The bandwidth of the sample may range from a few megahertz down to 1Hz. At gigahertz frequencies, small bandwidths are virtually impossible to create; the quality (Q) factor of a filter at 1GHz with a 1Hz bandwidth is $1 \cdot 10^9$. Even if such a high Q filter could be made, it would not be tunable and the cost would be overwhelming. In order to accomplish the task of sampling very small bandwidths, the spectrum analyzer is implemented as a triple heterodyne tuned receiver. Figure 1.1 shows the block diagram of a modern high performance spectrum analyzer.

In the first stage the input signal is mixed with a tunable 4GHz to 7GHz local oscillator (LO). The lowpass filter after the input blocks all LO feedthrough through the first mixer. Even a small LO signal at the input of the spectrum analyzer could interfere with an oscillator being tested. The output of the first mixer is filtered

by a narrowband 4GHz filter. This filter typically has a bandwidth of 50MHz. The output of the 4GHz filter is mixed with a fixed frequency oscillator of 3.7786GHz and then filtered. This second filter is at 221.4MHz and typically has a bandwidth of a few megahertz. The signal is downconverted a final time to 21.4MHz and filtered with a selection of narrowband filters. These are electronically switchable and is where the bandwidth (BW) selection of the spectrum analyzer takes place. After this selection, the signal is sent through a logarithmic amplifier and sampled by an analog to digital (A/D) converter to be processed and sent to a display.

The first oscillator is one of the more critical items with respect to performance. The most important performance parameter is it's phase noise. This is a measure of how pure the sinusoid is being generated by the oscillator. A more recent, and almost as important, parameter of the oscillator is it's tuning speed. Modern spectrum analyzers generally use high quality but rather slow tuning ferromagnetic oscillators also known as yttrium-iron-garnet (YIG) oscillators [1]. On the other hand, modern communication systems may use frequency hopping techniques which require ultrafast frequency changes not attainable with current YIG technology. Therefore, the past few years have seen a rise in the use of varactor tuned oscillators in low frequency measurement equipment. However, the operating frequency of frequency hopping systems is increasing and thus there is a need to design high performance and high frequency varactor tuned oscillators with broad tuning capability.

1.3 Oscillator Performance Parameters

Previously discussed is the use of a wideband oscillator in modern measurement equipment. Now it is important to look at all the major specifications required of an oscillator. Topics of interest to engineers who use oscillators are performance

parameters such as frequency tuning range, output power, noise specifications, modulation bandwidth and tuning speed.

Frequency tuning range is one of the most fundamental tradeoffs in an oscillator, impacting both the technology and topology used. The Q factor of the resonator sets the noise performance of the oscillator. In general, the more tunable an oscillator is, the lower the Q of the resonator. A wideband oscillator will usually use either a YIG element or a varactor as the tunable element in the system.

Noise specifications define the quality of the signal generated by the oscillator. This includes short term and long term phase and amplitude stability. Long term phase stability is not a critical parameter in varactor oscillators as they are usually used in a phase-locked-loop with a known precision oscillator at a lower frequency. Long term amplitude stability is the drift in output power of the oscillator over a period of time due to factors such as changes in temperature. Short term amplitude stability is known as amplitude modulation noise or AM noise. In general, this is much less critical than phase fluctuations of an oscillator and is usually measured in prototyping but generally not specified.

Short term phase stability is known as phase noise. A perfect sinusoidal output of an oscillator would have identical time between subsequently measured zero crossings along the time axis. Any deviation from this time is defined as a phase fluctuation. Phase noise is measured as the power spectral density of the phase fluctuations and is specified as the amount of power in a 1Hz BW referenced to the carrier (dBc) at some offset frequency (f_m).

Figure 1.2 is a comparison between three high performance, octave tuning oscillators. Koji Harada of Agilent Technologies designed a 0.75GHz to 1.5GHz varactor tuned oscillator with a phase noise of -117dBc at a 10kHz offset at 1GHz [2]. The 3GHz to 7GHz YIG tuned oscillator is commonly used in measurement equipment and exhibits a phase noise of -105dBc at a 10kHz offset at 5GHz. Tom Higgins

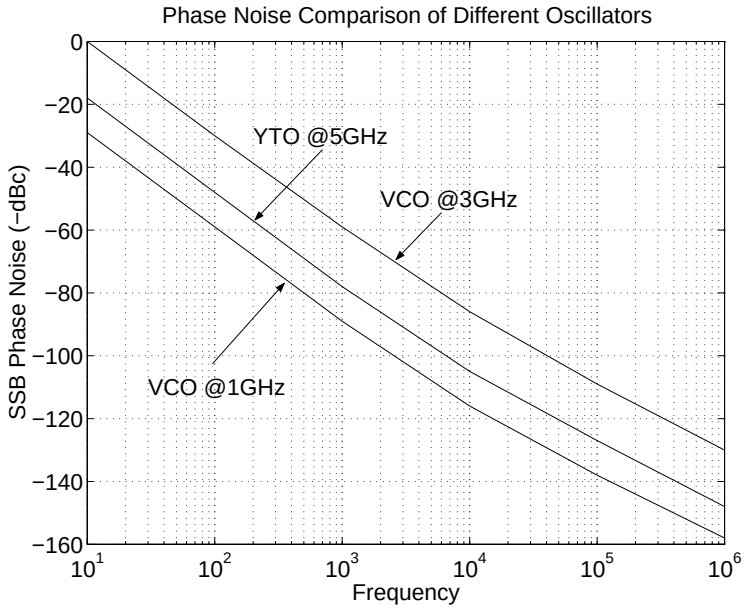


Figure 1.2. Phase noise comparison for a high performance 0.75GHz to 1.5GHz oscillator, a 1.5GHz to 3GHz oscillator and a 3GHz to 7GHz YIG tuned oscillator.

of Agilent Technologies designed the 1.5GHz to 3.0GHz varactor tuned oscillator which has a phase noise of -85dBc at a 10kHz offset at 3GHz.

The importance of an oscillator's noise performance is apparent after analyzing how information is modulated onto a carrier. Frequency and phase modulation both store information in reference to the carrier so that the noise of the oscillator within the modulation bandwidth sets the signal to noise ratio of the modulation system.

For example, in Quadriture Phase Shift Keying (QPSK) modulation, digital data is encoded by the amount of shift of phase from the reference carrier signal. If a perfect sinusoid was QPSK modulated then only four dots would appear in the IQ constellation diagram of Fig. 1.3. Phase noise of the carrier will spread the dots (data) along a constant radius circle. AM noise is shown as a change in the magnitude of the radius. The effects due to phase noise on digital communication systems is discussed and analyzed in [3] and [4].

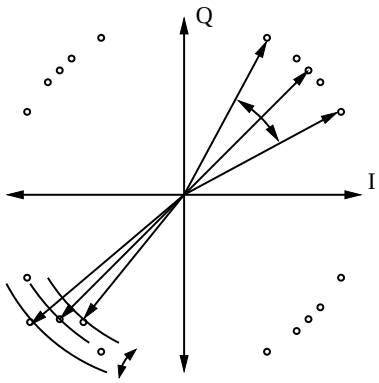


Figure 1.3: IQ diagram with presence of phase and amplitude noise.

Modulation bandwidth concerns the ability of an oscillator to be accurately modulate by a FM signal driven at its tuning port and it is typically described as the point where FM modulation at the output of the oscillator is reduced in amplitude by 3dB. The modulation bandwidth of an oscillator can be on the order of 100kHz to 10MHz.

The tuning speed is a measure of how fast the oscillator can change from one frequency value to another. While this parameter does not affect fixed frequency systems or systems with little tuning it is critical to frequency hopping systems, radar and measurement instrumentation.

1.4 Oscillator Technologies

Commercial wideband microwave oscillators operating at frequencies between 2GHz and 50GHz are typically designed using YIG elements. YIG oscillators tune between an octave and a decade of frequencies and demonstrate excellent phase noise due to the extremely high Q of the YIG resonator [1].

However, YIG oscillators are costly and difficult to design and manufacture. Tuning is accomplished by a large DC magnetic field, resulting in high current consumption. Tuning speed is limited by the time it takes to tune the DC magnetic

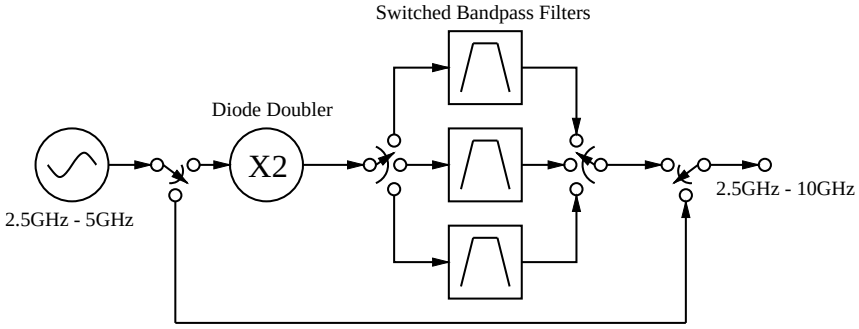


Figure 1.4. Octave tuning oscillator implemented in a 2.5GHz - 10GHz microwave synthesizer.

field to a new value.

At frequencies below 2GHz, wideband tunable oscillators based on variable-capacitance diodes (varactors) have demonstrated excellent performance, offering good phase noise, octave frequency tuning and extremely low cost. Above 2GHz, varactors have seen limited use in wideband tunable oscillators due to their reduced Q factor.

1.5 Focus of Work

Microwave instrumentation is in need of an octave tuning microwave oscillator capable of YIG-like phase noise with improved frequency tuning speed and lower cost. A varactor oscillator tunable between 2.5GHz and 5GHz may be implemented as a 2.5GHz to 10GHz replacement for a YIG oscillator using a broadband frequency doubler and switched filter bank to remove harmonics as shown in Fig. 1.4.

The goal of this work is to extend the current frequency range of octave tuning varactor oscillators for use in microwave instrumentation and to present the design in a clear and concise manner. This thesis presents the design, simulation and measurement of an octave tuning osctillator centered at 3GHz. This oscillator was implemented into a modern integer-n phase-locked-loop Chapter 7 summarizes

the performance, both predicted and measured, of this oscillator and presents a theoretical analysis of phase noise improvements by implementation of a frequency discriminator.

CHAPTER 2

OSCILLATOR THEORY

2.1 Theory of Operation

An oscillator is fundamentally an amplifier with a frequency selective positive feedback which has a magnitude greater than one and phase shift equal to a multiple of 2π around the loop. The basic topology for an oscillator is shown in Fig. 2.1 where A is the gain of the amplifier and β the transfer function of the feedback network. The gain of the closed loop system is written as 2.1 [5]. As the term AB approaches unity and is real, the gain diverges and it is possible to have a finite signal at the output even without a finite signal at the input. The feedback system has become an oscillator.

$$A_{CL} = \frac{A}{1 - A\beta} \tag{2.1}$$

In reality, an open loop gain Aβ greater than one is necessary to start the oscillation. The oscillator will reach steady state when the large signal non-linearities

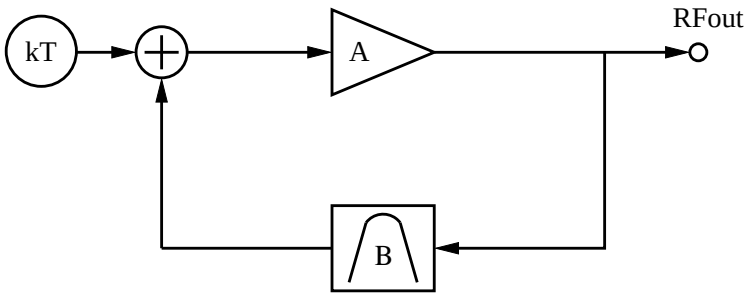


Figure 2.1: General function of an oscillator.

of the amplifier limit the product of Aβ to unity. The two conditions that must be met for steady state oscillation are $|A\beta| = 1$ and $\angle A\beta = 2\pi$.

In order for a closed loop system to be tunable, some element must be variable in order to achieve feedback at a different frequency. The frequency selective feedback of an oscillator is usually a resonator, which can be modeled as an LCR tank circuit in either a parallel or series configuration. A tunable oscillator will vary one of the parameters that set the oscillation condition in order to change the oscillation frequency. The value of the inductor or capacitor may be varied to change the oscillation frequency.

2.2 Common Oscillator Topologies

Most wideband varactor tuned oscillators are a variation of the Colpitts or Hartley oscillator, commonly analyzed as negative resistance topologies [6] [7]. The Colpitts and Hartley oscillators will be referred to here as a common emitter oscillator and a common base oscillator, respectively. The common emitter oscillator, shown in Fig. 2.2 uses a capacitive feedback network with C1 and C2 to create a negative resistance looking into the base of the transistor [7]. The common base oscillator, shown in Fig. 2.3 uses an inductor in the base of the transistor to create a negative resistance looking into the emitter of the transistor [8]. The resonator will have some positive resistance. Oscillation occurs when the absolute value of the negative resistance looking into the active device is greater than the absolute value of the positive resistance of the resonator [7].

Negative resistance theory accurately predicts the oscillation frequency and the ability of an oscillator to oscillate by simple calculation of the center frequency and loss of the resonator and negative resistance of the transistor. However, calculation of the loaded Q factor of the negative resistance topology without some

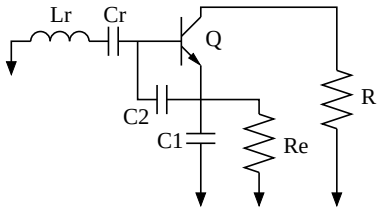


Figure 2.2: Common emitter negative resistance oscillator.

transformation is difficult. The load seen by the resonator is negative and the resulting loaded Q would be infinite if taken in this context [9]. Other analysis done using negative resistance simply neglect loaded Q as in [10]. Loaded Q is found as a measured quantity but not predicted in [11]. Another method must be used to predict and optimize loaded Q in a negative resistance topology for low noise design.

2.3 Transforming One-Port to Two-Port Topology

Most negative resistance oscillators employing a three terminal active device may be redrawn into a two port network using the concept of a virtual ground [8] [12]. This will allow use of the small signal model for the transistor and enable analysis of the loaded Q of the resonator.

Transistor S-parameters are usually given in the common emitter amplifier configuration and can be transformed to a common base configuration as shown in [13]. Rearranging the negative resistance oscillator to a two port and analyzing as a two port network allows easy ccalculation of the loaded Q.

The common-emitter negative resistance oscillator is shown in Fig. 2.4(a).

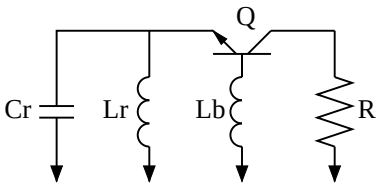


Figure 2.3: Common base negative resistance oscillator.

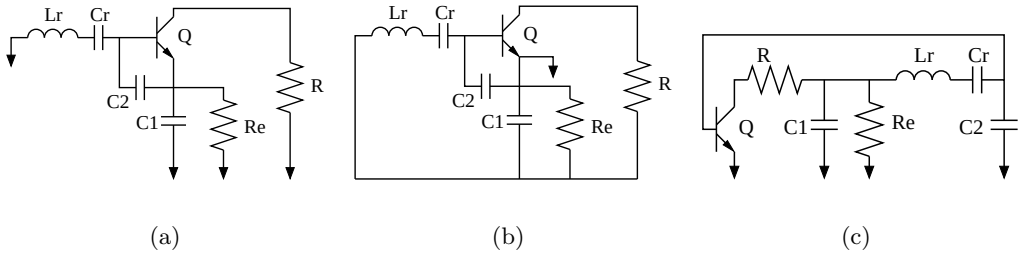


Figure 2.4. Negative resistance common emitter to 2-port transformation using a virtual ground.

A virtual ground is introduced at the emitter of the transistor and the true ground is drawn as a connected signal path in Fig. 2.4(b). The schematic is then redrawn to show the amplifier and resonator as separate two port networks in Fig. 2.4(c). The two port networks can be analyzed using measured S-parameter data of the amplifier and resonator or a small signal model may be substituted in place of the transistor. The second method is preferred as it allows simple analysis of the loaded Q of the system.

The common base negative resistance oscillator shown in Fig. 2.5(a) may also be redrawn as a two port network. A virtual ground is introduced in Fig. 2.5(b) at the base of the transistor and the true ground closed as a signal path. The schematic is redrawn as a two port configuration with a common base amplifier in Fig. 2.5(c). Again measured s-parameters of the transistor and resonator may be used or the system may be analyzed using a small signal model for the transistor. The latter approach here allows easy calculation of the loaded Q of the system.

Substituting the small signal model in place of the BJT is advantageous in both the common emitter and common base topologies. The benefit of this analysis is selection of the load resistance for the optimum loaded Q. Figures 2.6(a) and 2.6(b) show the 2-port common emitter and common base topologies with small signal transistor models, respectively. The loading of the resonator for the common emitter case is due to the series combination of the load, base and emitter resistance

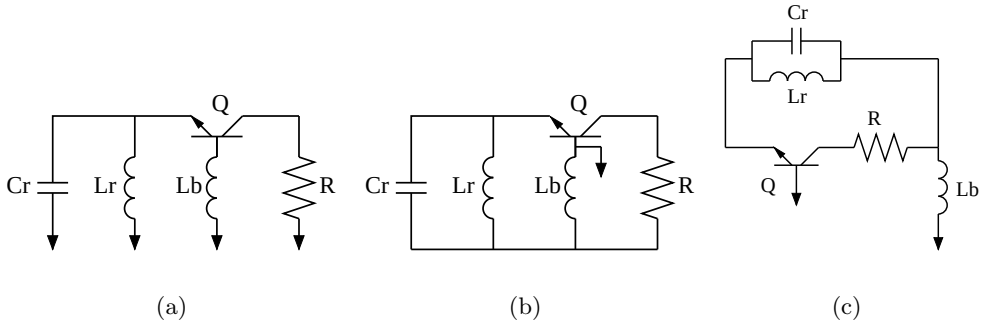


Figure 2.5. Negative resistance common base to 2-port transformation using a virtual ground.

and the parallel capacitance of C1 and C2. Small values of C1 and C2 create large negative resistance and allow broad tuning of the oscillator at the expense of heavily loading the resonator. Large values of C1 and C2 raise the loaded Q of the resonator at the expense of less tuning range and lower negative resistance. This topology is best suited for narrow tuning oscillators.

The resonator in the common base topology shown in 2.6(b) is loaded only by the series combination of the load resistance and the $\frac{1}{g_m}$ of the transistor. The loaded Q of the resonator is unaffected by the negative resistance and is therefore better suited to wide tuning range. The common base topology was chosen for this reason.

2.4 Tuning Range

Tuning range of the oscillator is determined by the amount the LC tank circuit has the ability change resonant frequency and how strongly it is coupled. The frequency of oscillation of a tank circuit is defined as $\omega_0 = \frac{1}{\sqrt{LC}}$. An octave tuning oscillator will need minimum capacitive tuning range of 4:1.

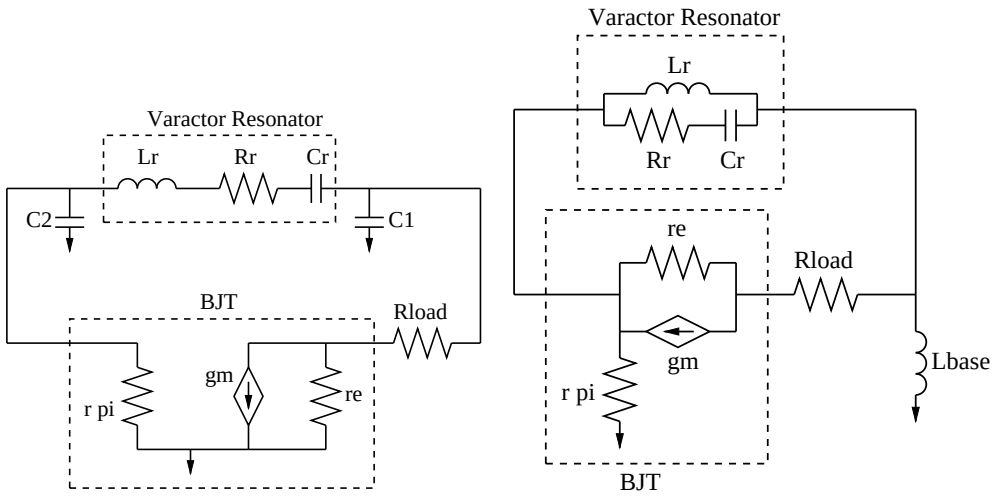


Figure 2.6. Small signal 2-port oscillator diagrams for the common emitter 2.6(a) and common base 2.6(b) topologies.

2.5 Output Power

Output power is determined by the power saturation properties of the amplifier and how far into compression it is. The difference in gain of the amplifier at startup (small signal) and the gain of the amplifier in steady state oscillation (large signal) defines the amount of compression the amplifier is in. The amount of compression will be a gauge of how much output power the amplifier will be producing. Using this technique, the output power of the oscillator may be predicted by knowing the loss of the resonator and small signal gain of the amplifier, the difference being the amount of compression the amplifier will be in steady state.

2.6 Phase Noise

Phase noise is measured as the power spectral density of the phase fluctuations of a sinusoid. The application note from Hewlett-Packard on phase noise characterization in microwave oscillations [14] gives an excellent definition of phase

noise and will be summarized here.

A noiseless sinusoid can be described by 2.2, while a real signal with noise can be described by 2.3 where $\epsilon(t)$ represents the amplitude fluctuations and $\Delta\phi(t)$ represents the phase fluctuations. Equation 2.4 shows an approximation of the relation between the phase fluctuations and their power spectral density where f_m is some offset frequency from the carrier.

$$v(t) = V_0 cos(2\pi f_0 t) \tag{2.2}$$

$$v(t) = (V_0 + \epsilon(t))cos(2\pi f_0 t + \Delta\phi(t)) \tag{2.3}$$

$$S_\phi(f_m) = \frac{\Delta\phi^2_{rms}(f_m)}{\text{BW used to measure } \Delta\phi_{rms}} \tag{2.4}$$

The National Institute of Standards and Technology (NIST) define $\mathcal{L}(f_m)$ as the ratio of the power in one phase modulation sideband at an offset frequency f_m from the carrier to the total signal power. This is related to the power spectral density S_ϕ by Eq. 2.5. $\mathcal{L}(f_m)$ is normalized to a 1Hz BW.

$$\mathcal{L}(f_m) = \frac{1}{2} S_\phi(f_m) \tag{2.5}$$

Leeson developed a simple model of the oscillator noise spectrum in [15] and is analyzed more closely in [16] [17] [18]. In an oscillator, PM noise is generally much larger than AM noise and so the latter may be neglected so the remainder of this analysis will use phase noise only. AM noise is suppressed in an oscillator by the compressed condition of the amplifier. Some systems, such as radar, may require

more stringent standards of AM noise and so must be considered in a separate AM noise analysis.

The phase noise of an oscillator is analyzed first as an open loop and then a closed loop system. In the open loop system the noise of the amplifier dominates. The noise due to the amplifier is shown in Eq. 2.6 as a signal to noise ratio where P_o is the power of the oscillator at the point where it will be measured (usually the output), k is Boltzmann's constant, T is the absolute temperature in Kelvins and F is the noise factor of the amplifier. In a truly random system the noise will be composed of equal AM and PM components. This analysis deals with PM noise only so the noise power is reduced by half.

$$S_\phi|_{thermal} = \frac{kTF}{P_o} \tag{2.6}$$

Equation 2.6 is derived in Eqs. 2.7 to 2.11. Equation 2.7 shows the voltage noise due to the thermal noise of a resistor. This is voltage divided to a load of resistance R_L and has maximum power transfer when $R = R_L$ in 2.8. Equation 2.7 and 2.8 are peak voltages. The voltage at the load R_L is converted to an rms power in Eq. 2.9 and is shown to be equal to kT. This noise power is due to equal parts AM and PM noise and so is divided by 2 in 2.10. The power spectral density is a ratio of the noise power to signal power, P_o as shown in Eq. 2.11. S_ϕ is a double sideband measurement and is therefore multiplied by a factor of 2.

$$V_n = \sqrt{4kTR} \tag{2.7}$$

$$V_n|_{load} = V_n \frac{R_L}{R + R_L} \tag{2.8}$$

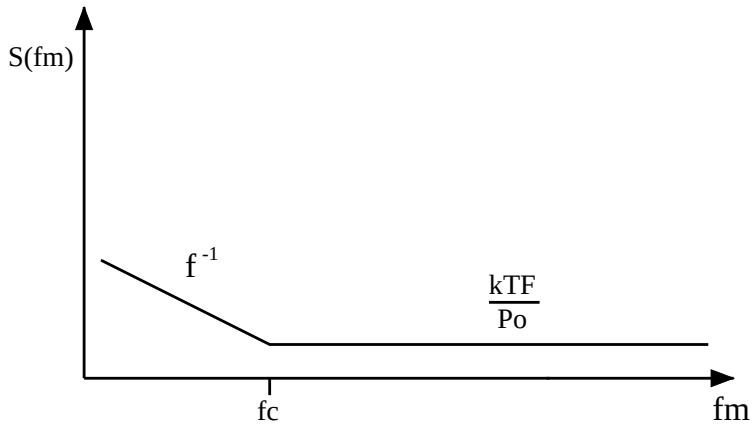


Figure 2.7: Flicker and thermal noise of an amplifier.

$$P_n|_{load(rms)} = \frac{V_n^2|_{load}}{2R} = kT \tag{2.9}$$

$$P_n|_{phase\ noise} = \frac{kT}{2} \tag{2.10}$$

$$S_\phi|_{double\ sideband} = \frac{2P_n|_{load}}{P_o} = \frac{kTF}{P_o} \tag{2.11}$$

Amplifiers also exhibit a noise known as flicker noise. This is a near DC noise that is proportional to $\frac{1}{f}$ and increases as the frequency decreases [19]. This noise is evident at frequencies closer to the carrier than the flicker corner, f_c. The power spectral density is rewritten to show this effect in Eq. 2.12. The total noise contributions of the amplifier can be seen graphically in Fig. 2.7.

$$S_\phi|_{amp} = \left(\frac{kTF}{P_o}\right)\left(1 + \frac{f_c}{f_m}\right) \tag{2.12}$$

The closed loop phase noise is the noise due to the amplifier in the presence of a frequency selective feedback with finite bandwidth or Q factor. The Q factor

of a resonator is defined as the center frequency of resonance f_0 divided by the half power (-3dB) bandwidth (BW) as shown in Eq. 2.13. The phase noise due to the finite Q factor of the resonator, at an offset f_m from the carrier, is described by Eq. 2.14 where Q_L is the Q factor of the resonator as loaded by the oscillator.

$$Q = \frac{f_0}{BW} \tag{2.13}$$

$$S_\phi(f_m) = \left(1 + \frac{f_0^2}{(2f_m Q_L)^2}\right) S_\phi(f_m)|_{amp} \tag{2.14}$$

The total phase noise of the closed loop system is described by Eq. 2.15, normalized to a 1Hz bandwidth. The phase noise characteristics of an oscillator are shown graphically in Fig. 2.8. The power spectral density is rewritten in Eq. 2.16 as a single sideband measurement. $\mathcal{L}_\varphi(f_m)$ is the phase noise value that will be referenced throughout this thesis.

$$S_\varphi(f_m) = 10\log_{10}\left[\left(1 + \frac{f_0^2}{(2f_m Q_L)^2}\right)\left(1 + \frac{f_c}{f_m}\right)\left(\frac{kTF}{P_o}\right)\right] \tag{2.15}$$

$$\mathcal{L}_\varphi(f_m) = 10\log_{10}\left[\left(1 + \frac{f_0^2}{(2f_m Q_L)^2}\right)\left(1 + \frac{f_c}{f_m}\right)\left(\frac{kTF}{2P_o}\right)\right] \tag{2.16}$$

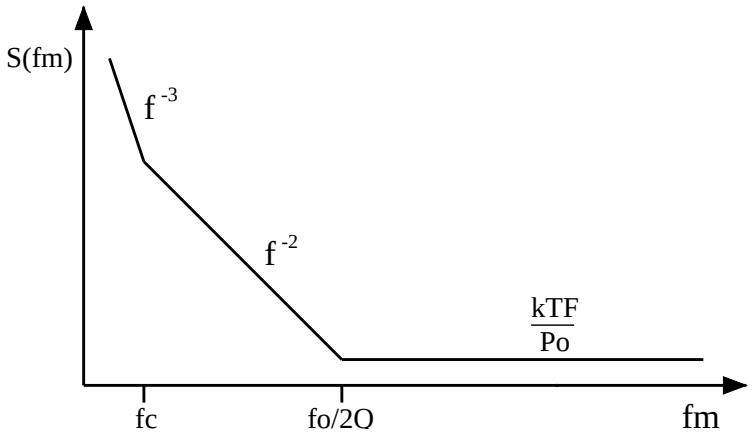


Figure 2.8: Phase noise characteristics of an oscillator.

CHAPTER 3

ACTIVE DEVICES

3.1 Function

The amplifier provides both the output and feedback power to sustain the oscillation condition. While it is easy to turn virtually any amplifier into an oscillator, it is much more difficult to make one into a very good oscillator. This section will summarize the specifications and properties of amplifiers that operate optimally in an oscillator designed for 2.5GHz to 5GHz operation.

The three main properties of an amplifier that must be carefully considered are noise, power output and gain at the desired frequency. The amplifier will contribute to the oscillator's noise with three kinds of noise, thermal, shot and flicker. The thermal and shot noise affect the signal to noise ratio far from the carrier while the flicker affects the oscillator noise close to the carrier. One of the most important tradeoffs in amplifier is between gain and power output. The gain of an amplifier is limited by the process. A common measure of the limit is known as the transition frequency (f_t) or gain bandwidth product (GBW). Power output can be determined by increasing the device size. Power output and gain are carefully balanced to provide the optimum performance.

All three of these parameters are heavily dependent on the transistor process and technology type. Common processes are silicon (Si), gallium arsenide (GaAs) and silicon germanium (SiGe). Typical technologies used are bipolar junction transistor (BJT), field effect transistor (FET) and heterojunction bipolar transistor

(HBT). There are many more to choose from, these are the most commonly used.

3.2 Noise

Noise comes in three forms: thermal noise, shot noise and flicker noise. Thermal noise is caused by the thermal excitation of charge carriers in a conductor and has a white power spectral density. The noise due resistance in the amplifier described by Eq. 3.1 where B is the bandwith. Any internal resistances within the transistor will add to the thermal noise, decreasing the signal to noise ratio of the oscillator.

$$V_n(f) = \sqrt{4kTRB} \tag{3.1}$$

The second kind of noise is shot noise. This is seen in PN junctions from the current being a discrete flow of carriers. Shot noise is depedent on the DC current value flowing through the PN junction. Shot noise can be modeled as white noise. To some degree, the contribution of shot noise can be reduced by lowering the DC bias current. This reduction is limitated by the transconductance gain g_m being proportional to the DC bias current.

The third noise is called flicker noise. This is the least understood of the three. It has the property of increasing in value as the frequency decreases as described in Eq. 3.2 where K_V is a constant. Flicker noise arises due to traps and impurities in the semiconductor where carriers are held for some time then released rather than traveling through the device [19] [20] [21]. Reference [19] provides a measurement and simulation method for flicker noise. Flicker noise is parametrically upconverted to the fundamental frequency of oscillation.

$$V_n(f) = \frac{K_V}{\sqrt{f}} \tag{3.2}$$

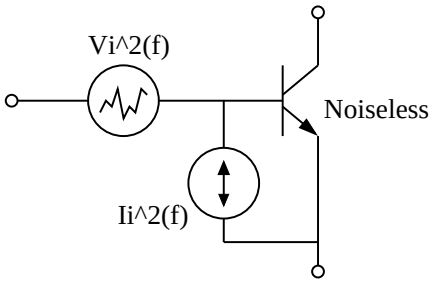


Figure 3.1: Noise Model for a BJT Device

The noise model for a BJT device is shown in Fig. 3.1 [20]. Equation 3.3 describes the voltage noise source in terms of the device parameters. Here it can be seen that the noise voltage of the device is depedent on the base resistance (r_b) and the transconductance (g_m). The transconductance g_m is calculated by Eq. 3.4.

$$V_n^2(f) = 4kT\left(r_b + \frac{1}{2g_m}\right) \tag{3.3}$$

$$g_m = \frac{I_C}{V_T},\ V_T = \frac{kT}{q} \tag{3.4}$$

The noise current is described in Eq. 3.5 where q is the elctron charge, I_B is the DC base current, I_C is the DC collector, K is the flicker noise scaling constant, β is the is current gain of the device and f is frequency. The noise current is dominated by the base current shot noise proportional to $2qI_B$ and the flicker noise described in the term $\frac{2qKI_B}{f}$. The term $\frac{2qI_C}{|\beta(f)|^2}$ is the collector shot noise from the DC collector current and is relatively insignificant.

$$I_n^2(f) = 2q(I_B + \frac{KI_B}{f}\frac{I_C}{|\beta(f)|^2}) \tag{3.5}$$

The noise of an oscillator can be measured as a noise factor (F) and is defined by the Eq. 3.6 [22]. as the ratio of the signal to noise ratio at the input to

the signal to noise ratio at the output. The noise factor depends on the thermal and shot noise of the amplifier. The noise factor is commonly used in a log scale and is then called noise figure (NF). A low noise figure device generally has a low base resistance, R_b, low current consumption and poor 50Ω match.

$$F = \frac{Si/Ni}{So/No} \tag{3.6}$$

Noise figure is measured by a method known as the Y-factor method [23]. It is inherently a linear, small signal measurement. When an amplifier is measured in compression, the noise figure is increased by the same amount of compression the amplifier is in. The signal to noise ratio of an oscillator is reduced by the amount indicted by the noise figure.

3.3 Processes and Technologies

Of the three processes given in section 3.1 (Si, GaAs and SiGe), Si has the lowest f_t of the three and is commonly used in sub 10GHz oscillators. The highest frequency devices are presently made in a $f_t = 25GHz$ or $f_t = 45GHz$ process. Agilent Technologies and Siemens Semiconductor both manufacture devices these processes. NEC has a $f_t = 15GHz$ process. The silicon process generally has the lowest impurities due to the single element crystaline structure and therefore the lowest flicker noise. BJT's are the most common type of oscillator amplifier made in silicon. FETs exhibit more noise and less gain than BJTs in silicon and are therefore not preferred for low noise and high frequency designs.

GaAs has a very high electron mobility which equates to lower capacitance and higher f_t than Si. However, the GaAs process is not as pure, leading to a higher flicker noise. FETs used at high frequencies are generally designed into a GaAs process. Many modern sub-mm range amplifiers are Heterojunction Bipolar

Junction Transistors (HBT) made in the GaAs process. The HBT process exhibits a lower flicker noise corner f_c than FETs.

SiGe is relatively new and has seen little use in oscillator design. A SiGe BJT usually has a very low NF and moderate flicker noise corner with an f_t between that of Si and GaAs.

Oscillators under 10GHz are generally Si BJT devices. They offer low noise figure and flicker corner f_c, good gain and good power output. The Agilent Technologies $f_t = 25GHz$ was chosen for these properties. Three devices are available in this process listed from highest to lowest gain: hbfp-0405, hbfp-0420 and hbfp-0450 [24] [25] [26]. Power output is listed from lowest to highest, respectively. The highest frequency of operation for this oscillator will be 5GHz. At 5GHz, the associated gain is 12dB, 10dB and 7dB, respectively. The respective noise figures are 2.5dB, 2.8dB and 2.5dB. The 1dB compression point (specified at 2GHz) is 5dBm, 12dBm and 15dBm respectively. The hbfp-0420 is the best compromise between low noise figure, output power and available gain. The remainder of the simulations and measurements were done with this transistor.

3.4 Nonlinear Model

While the datasheets provided a quality nonlinear model and measured S-parameters, it is important to measure the device in the actual environment and bias conditions it will be used in to verify the model. Two configurations were measured, the common emitter and common base amplifier. The common base will use an inductor in the base and will be analyzed as a negative resistance device.

3.5 Common Emitter Measurements

S-parameters were measured with the hbfp-0420 amplifier in a grounded common emitter configuration. The plastic packaged part was mounted on a 10mil

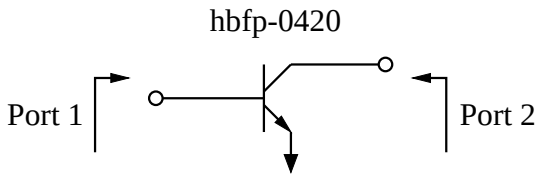


Figure 3.2: Measurement setup for the common emitter amplifier measurements.

thickness Rogers 4350 substrate with a two 20mil vias to ground, one via 30mils from each emitter pin. The hand assembly and copper milled PCB limited the proximity and number of vias to the emitter pads. The 8510 network analyzer was set to a power output of -10dBm (measured) for a small signal measurement. The test board was measured on the network analyzer and the electrical delay adjusted to reference the measurements at the end of the pads of the device. The measurement configuration is shown in Fig. 3.2.

The amplifier was measured for values of I_C=10mA, 15mA and 20mA. Current below this had significantly reduced gain and only slightly better noise figure. The transconductance gain g_m and NF are strongly depedent on I_C [25]. The V_{CE} voltage may range from 1V to 3V and directly affects the p^{-1dB} compression point. The power output is very low below 2V so S-parameter measurements were taken for V_{CE} values of 2V, 2.5V and 3V. Figure 3.3 shows the magnitude response from 1 to 10GHz over these nine bias conditions. As expected, the gain is the highest with the highest current. In comparison to the measured S-parameters provided in the datasheet, the measured parameters in Fig. 3.3 show a lower gain. This is due to the increased ground via inductance of the process that was available for prototyping the test fixtures.

Figure 3.4 shows the phase response over the same bias conditions. The importance of the S_{21} phase measurement lies in the need to know the bias voltage to phase coefficient. The phase is directly proportional to the center frequency of oscillation. Noise on the bias lines can cause additional phase noise if this coefficient

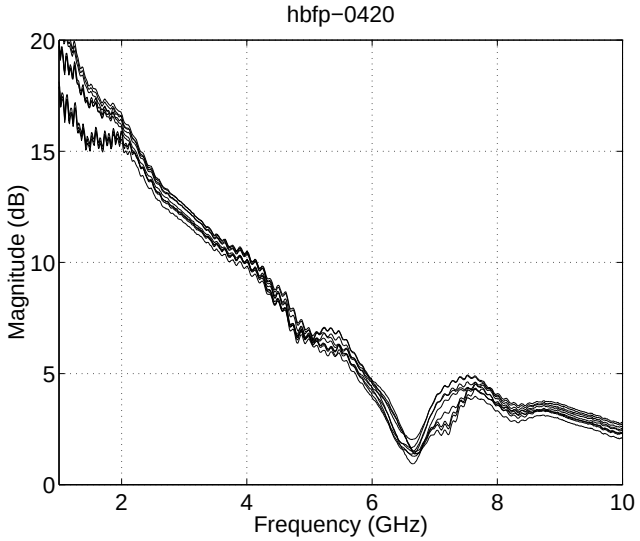


Figure 3.3. hbfp-0420 S_{21} magnitude response for different DC bias conditions: V_{CE} = 2V, 2.5V and 3V; I_C = 10mA, 15mA and 20mA.

is too large.

In the same fixture power compression curves were measured using an HP83650 microwave frequency source and a HP8565 spectrum analyzer. The system was calibrated using an HP438B power meter. These measurements were done in a 50Ω system.

Knowledge of the power and gain compression curves and related power output help in accurate prediction of the output power of an oscillator. Figure 3.5 shows the power output vs. power input characteristics of the hbfp-0420 device. It can be seen that even if in a mildly compressed state, the amplifier is producing 12dBm from 2 to 6GHz. This results in a relatively constant output power with frequency for an oscillator. Figure 3.6 shows the amount of gain compression vs. power input.

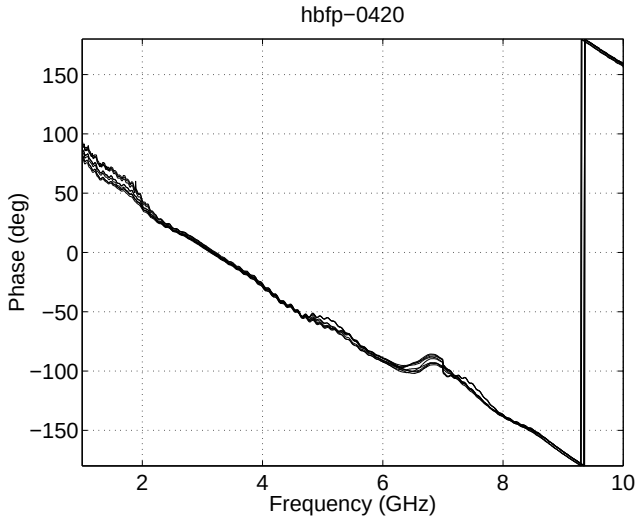


Figure 3.4. hbfp-0420 S_{21} phase response for different DC bias conditions: V_{CE} = 2V, 2.5V and 3V; I_C = 10mA, 15mA and 20mA.

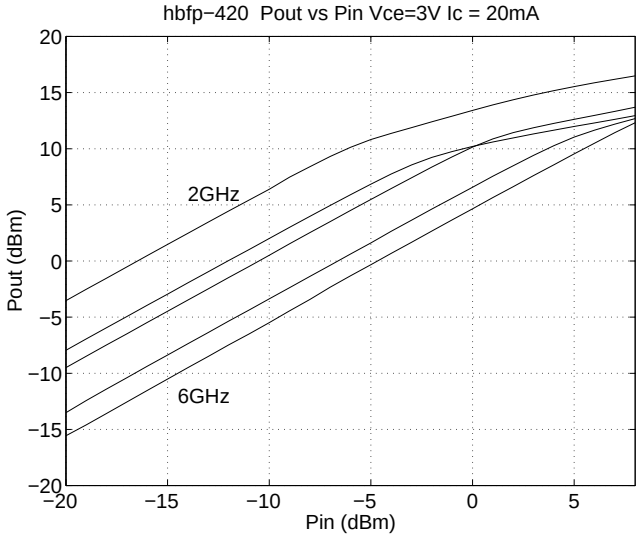


Figure 3.5. hbfp-0420 P_{out} vs. P_{in} for f=2GHz, 3GHz, 4GHz, 5GHz and 6GHz. V_{CE} = 3V and I_C = 20mA.

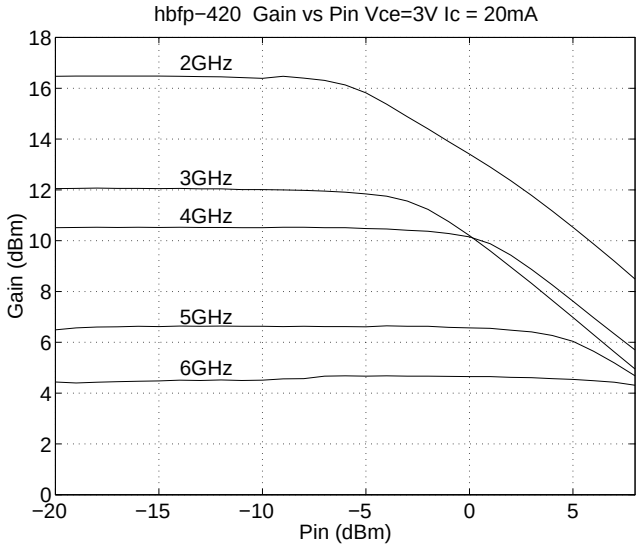


Figure 3.6. hbfp-0420 gain vs. P_{in} for for f=2GHz, 3GHz, 4GHz, 5GHz and 6GHz. $V_{CE} = 3$V and $I_C = 20$mA

3.6 Effect of Non-Linearities

The measurements shown above assume the device will be in the small signal mode. An oscillator is in steady state once the loop gain has been compressed to a magnitude of 1 and the phase is a multiple of 2π. At startup the loop gain is larger than 1 and the gain difference between startup and steady state is the amount the amplifier is in compression.

An amplifier in compression is no longer in the small signal mode and so the phase of S_{21} in the amplifier will change with respect to the amount of compression. It has been noted in references that for small amounts of compression, less than 3dB, the relative phase change is very small. This measurement verifies this general rule-of-thumb. An amplifier operating at a different phase shift than expected will result in the loop phase of 2π occuring at an offset from the center of the resonator pass band. This equates to an increase of phase noise. Figure 3.7 shows the phase difference between a power input of -10dBm and a power input of 5dBm. The data was taken for $V_{ce} = 3$V and $I_C = 20$mA.

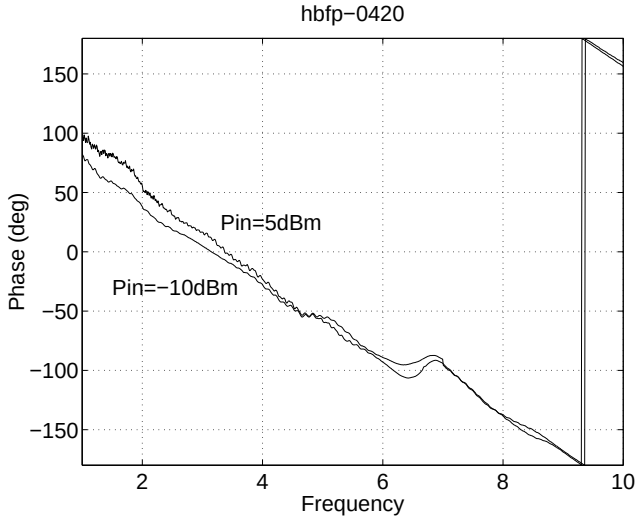


Figure 3.7. hbfp-0420 S_{21} phase response for P_{in} = -10dBm and P_{in} = 5dBm; V_{ce} = 3V and I_c = 20mA

3.7 Common Base Amplifier Measurements

Converting the common base oscillator topology to a 2-port network allows separation of the resonator and amplifier. Hence, the loaded Q and amplifier gain may be determined. However, the common base amplifier is still a negative resistance oscillator and it is important to set the base inductance value to provide a negative resistance across the band of interest. The measurement configuration is shown in Fig. 3.8.

Two inductance values are compared, 1nH and 3nH. The 3nH uses an air core commercial inductor for biasing, while the 1nH uses a short 3mm length of

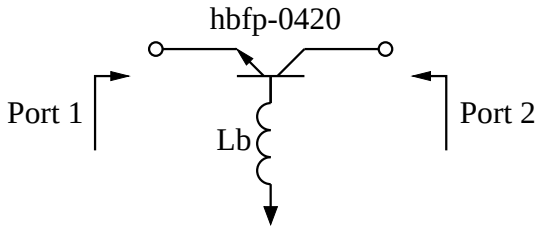


Figure 3.8. Measurement setup for common base amplifier measurements with base inductance.

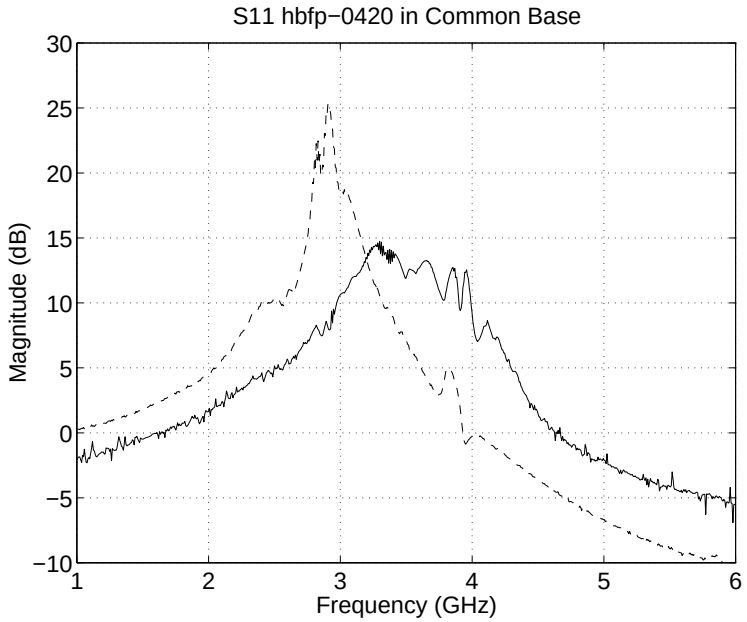


Figure 3.9. S_{11} of a common base amplifier with base inductance of 1nH (solid) and 3nH (dashed).

transmission line on the PC board. The negative resistance is measured as a S_{11} value greater than 0dB in Fig. 3.9. The 1nH inductor produces a 2.5GHz to 4.5GHz negative resistance while the 3nH inductance is optimum for a lower frequency. It can be seen that a slightly smaller inductance must be used to reach 5GHz. The S_{21} gain of the amplifier must also be greater than 0dB for proper operation. Figure 3.10 shows gain to 3.5Ghz for the 3nH inductor and to 4.6Ghz for the 1nH inductor.

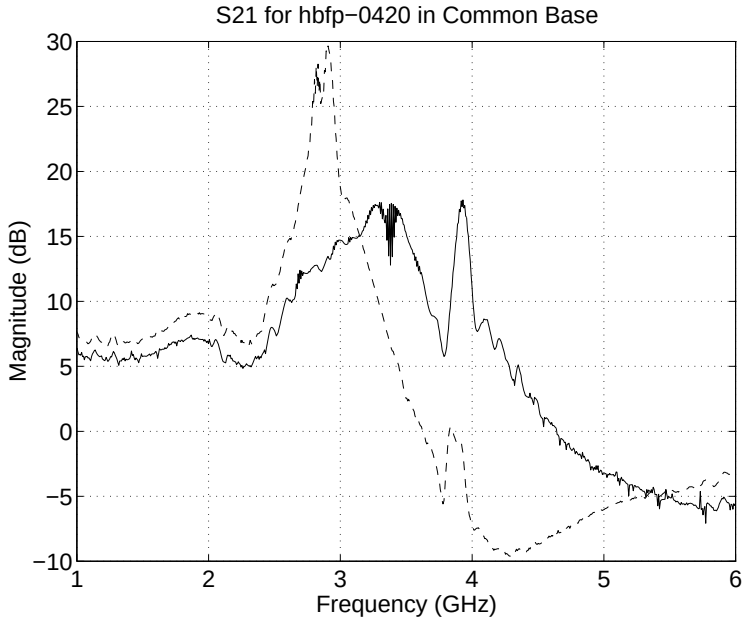


Figure 3.10. S_{21} of a common base amplifier with base inductance 1nH (solid) and 3nH (dashed).

CHAPTER 4

RESONATOR DESIGN

4.1 Function

The resonator has the most direct influence on the tunability and phase noise performance of an oscillator. The resonator, acting as the frequency selective feedback in the loop, determines the noise corner, proportional to $\frac{1}{Q_L^2}$, in the phase noise equation presented in 2.16 at which point the phase noise starts increasing at 20dB/decade as the offset frequency, f_m, goes towards zero. This chapter discusses the simulation and measurement of the parallel RLC resonator structure and the effects of varactor diode tuning.

4.2 Topology

The resonator is generally modeled as a series LCR or parallel LCR tank circuit. This depends on the topology of the oscillator used. A common base oscillator will typically use a parallel LCR resonator while a common emitter oscillator will use a series LCR. This design is based on the common base oscillator topology so a parallel LCR resonator will be evaluated. The parallel LCR resonator is shown in Fig. 4.1.

4.3 Loaded vs. Unloaded Q

Unloaded Q (Q_U) is a measure of the Q factor of an element or elements without the effect of any external circuit. The loaded Q (Q_L) is a measure of the

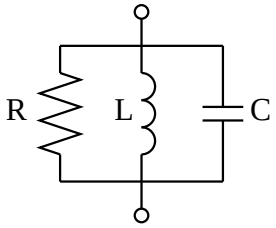


Figure 4.1: LCR parallel resonator.

Q factor of the element or elements when loaded by the environment in which it is used. The unloaded Q of an inductor, capacitor and resonator will be discussed first, followed by an analysis of the loaded Q of a system.

Q factor is a measure of the ratio between the amount of energy stored (X) and the energy dissipated (R) of a circuit as shown in Eq. 4.1, where $X = \frac{1}{\omega C}$ for a capacitor and $X = \omega L$ for an inductor. A non-ideal element will always have some resistance in series. The Q of a capacitor and resistor in series is calculated using Eq. 4.2. An inductor and resistor in series has a Q calculated using Eq. 4.3. The Q factor of a resonator, Q_R, with an inductor of Q_L and capacitor with Q_C is calculated by Eq. 4.4.

$$Q = \frac{X}{R} \tag{4.1}$$

$$Q = \frac{1}{wCR} \tag{4.2}$$

$$Q = \frac{wL}{R} \tag{4.3}$$

$$\frac{1}{Q_R} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{4.4}$$

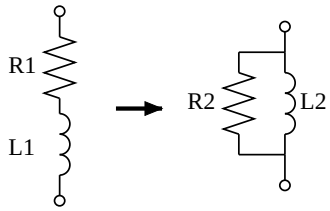


Figure 4.2. Conversion between a series LR model with finite Q to a parallel LR model with the same Q.

The series model for the inductor and capacitor with finite resistance may be converted into a parallel model as shown in Figs. 4.2 and 4.3 by Eqs. 4.5 and 4.6, respectively [27]. The parallel RC and LC circuits may be combined in parallel to form the LCR resonator model in Fig. 4.1 for convenience. The Q of a parallel LCR circuit is defined in Eq. 4.7.

$$L\|R \begin{cases} R2 = R1\left(1+Q^2\right) \\ L2 = L1\left(1+\frac{1}{Q^2}\right) \end{cases} \tag{4.5}$$

$$C\|R \begin{cases} R2 = R1\left(1+Q^2\right) \\ C2 = \frac{Q^2 C1}{1+Q^2} \end{cases} \tag{4.6}$$

$$Q = R\sqrt{\frac{C}{L}} \tag{4.7}$$

The LC resonator with finite Q elements may now be redrawn as an RLC resonant circuit within the 2-port small signal oscillator model presented earlier,

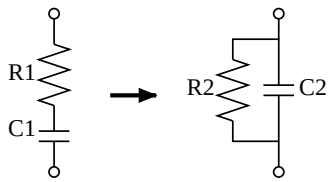


Figure 4.3. Conversion between a series CR model with finite Q to a parallel CR model with the same Q.

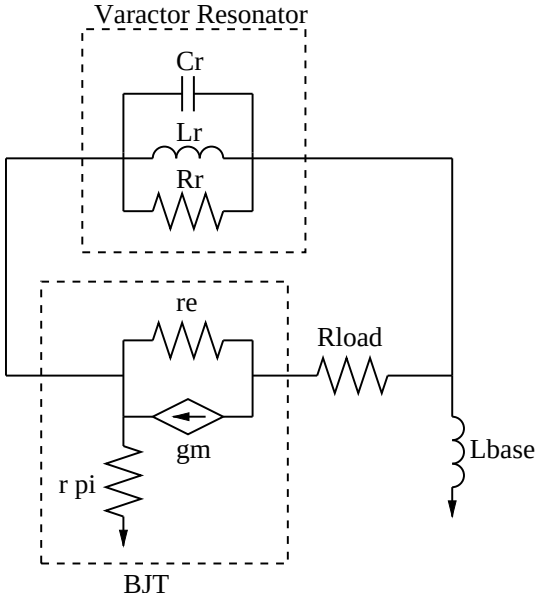


Figure 4.4: Small signal model of the 2-port resonator with a RLC resonator.

see Fig. 4.4. It can be seen here that the loaded resonator will have a resistance equivalent to R_r in parallel with the series combination of $\frac{1}{g_m}$ and R_{load}. This is the loaded Q of the resonator in the circuit.

The amount of loading on a resonator is very important for optimum phase noise in an oscillator. A very lightly loaded resonator will have a higher Q factor but will pass less power through it. A heavily loaded resonator will have a very low Q factor but will pass more power through it. The power transmission of the resonator is important as it affects the power output of the oscillator. The optimum loaded vs. unloaded Q is derived from Leeson's rule and the power transfer function of a 2-port parallel RLC resonator. Phase noise within the resonator BW is described by Eq. 4.8. Flicker noise effects have been removed for simplicity. The output power P_o has been replaced by the relation $P_o = GP_i$, where G is the gain of the amplifier.

$$S_\phi(f_m) = \frac{FkT}{GP_i}\left(\frac{f_0}{2Q_L f_m}\right)^2 \tag{4.8}$$

The power transfer function for an RLC resonator is shown in Eq. 4.9

where Q_E is the external Q factor of the system [28].

$$T = \frac{4Q_L^2}{Q_E^2} \tag{4.9}$$

The Q_L of the oscillator is the combination of Q_E and Q_U in the system as shown in Eq. 4.10. Let r be the ratio of Q_L and Q_U in 4.11 and solve for Q_E by substituting 4.11 into 4.10.

$$\frac{1}{Q_L} = \frac{1}{Q_U} + \frac{1}{Q_E} \tag{4.10}$$

$$r = \frac{Q_L}{Q_U} \tag{4.11}$$

$$Q_E = \frac{2Q_L}{1-r} \tag{4.12}$$

The power transferred by the resonator is equal to the power at the input of the transistor, P_i. Using Eq. 4.12 and Eq. 4.9, it is possible to write:

$$P_i = TP_o = P_o(1-r)^2 \tag{4.13}$$

Here the relation between the power at the input of the amplifier and the ratio between Q_L and Q_U can be seen. Substituting Eq. 4.13 and $Q_L = rQ_U$ from 4.11 into Eq. 4.8 relates the phase noise to the ratio between loaded and unloaded Q in 4.8. The variables indepedent of r can be combined as a constant K in 4.15 and rewritten as Eq. 4.16. This relation is plotted on a log scale in Fig. 4.5 and clearly shows the minimum phase noise is reached when $Q_L = 0.5Q_U$.

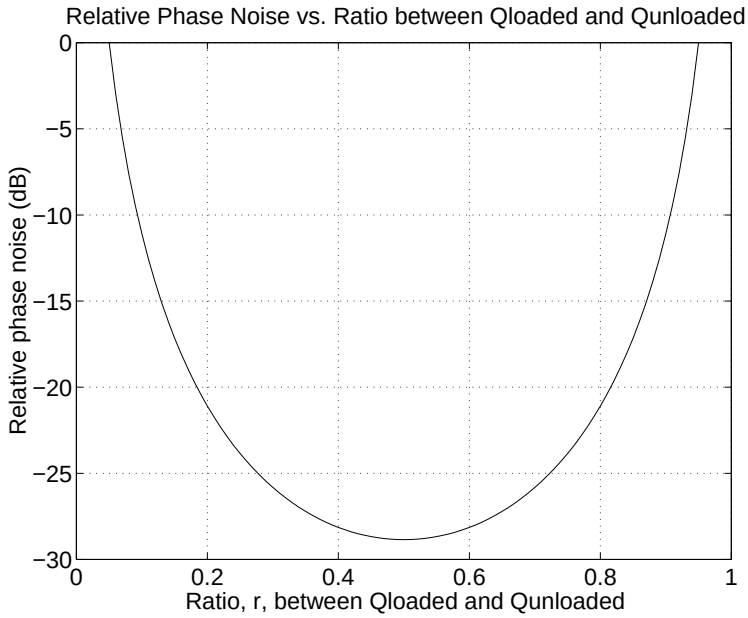


Figure 4.5: Relative phase noise vs. the ratio between the loaded and unloaded Q factor of a resonator, $r = \frac{Q_L}{Q_U}$.

$$S_\phi(f_m) = \frac{FkT}{GP_o(1-r)^2}\left(\frac{f_0}{2f_m r Q_U}\right)^2 \tag{4.14}$$

$$K = \frac{FkTf_0^2}{4GP_o f_m^2 Q_U^2} \tag{4.15}$$

$$S_\phi = K\frac{1}{r^2(1-r)^2} \tag{4.16}$$

4.4 Varactor

Varactors are usually the Q factor limitation in an LCR resonant circuit, where the varactor is the tunable element. Careful selection must be made to find the device with the highest Q for the frequency range of interest.

A varactor diode changes capacitance proportional to the reverse bias across the PN junction. Two common types of varactor diodes are abrupt and hyperabrupt. The abrupt junction varactor diode is made with a linearly doped PN junction and typically have a capacitance change of 4:1 or less over the specified range of reverse bias. Abrupt junction diodes are available with maximum reverse bias voltages between 5V and 60V. The higher voltages devices are advantageous as they lower the integration gain (MHz/V) of the oscillation but require a large supply voltage within the instrument. A hyperabrupt junction varactor diode has a non-linear doped PN junction that increases the capacitance change vs. reverse bias and may have a 10:1 capacitance change. The disadvantage of a hyperabrupt is higher series resistance and higher overall capacitance, lowering the Q. For high frequency and low noise oscillators, abrupt junctions are preferred.

Varactors may be manufactured in Si or GaAs. The GaAs process offers a varactor diode with lower capacitance for the same resistance due to the higher electron mobility than Si. Therefore the Q of a GaAs varactor is slightly higher than that of silicon. However, the flicker noise of a varactor made in GaAs is very high and would deteriorate the phase noise significantly. For this reason, only silicon abrupt junction diodes were considered for this design.

The varactor chosen for this oscillator is a Si abrupt from Toshiba, the 1SV280. This diode has a very low series resistance, low package parasitics and a tune range of 1V to 15V. The model representing a varactor diode is shown in Fig. 4.6. The diode series resistance, R_v, is reverse bias depedent and found from measurements presented in the datasheets. The R_v vs. reverse bias is plotted in Fig. 4.7. The junction capacitance C_j is calculated by Eq. 4.17 where C_{j0}=6.89pF, V_R is the reverse bias voltage and ϕ_0=0.7, the work function of silicon. The capacitance vs. reverse voltage is plotted in Fig. 4.8.

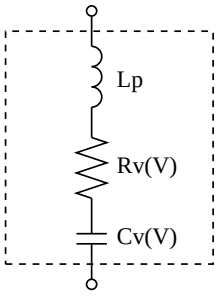


Figure 4.6: Varactor model with variable capacitance and resistance.

$$C_j = \frac{C_{j0}}{\sqrt{1 + \frac{V_R}{\phi_0}}} \tag{4.17}$$

The Q factor is calculated by Eq. 4.2 using the data from Fig. 4.7 and 4.8 is plotted for Q vs. reverse voltage in Fig. 4.9 for frequencies of 2GHz, 3GHz, 4GHz and 5GHz.

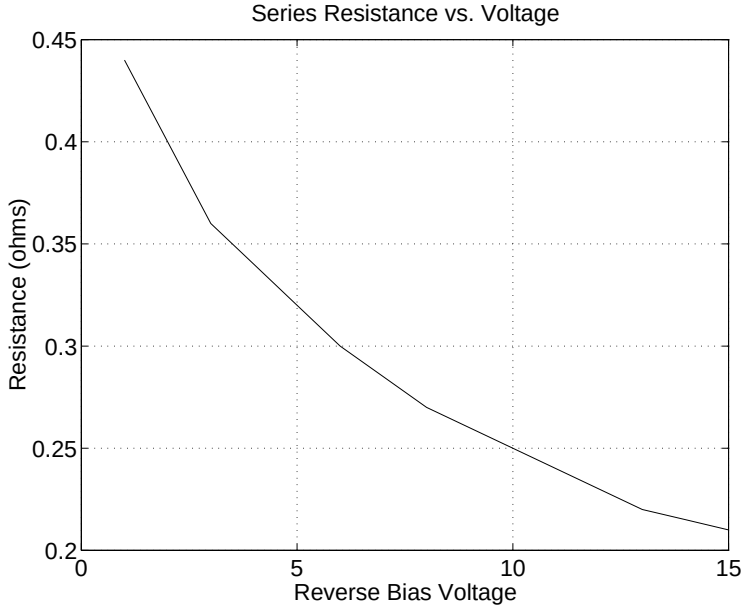


Figure 4.7. Resistance (Ω) vs. revsere bias voltage for the Toshiba 1SV280 varactor.

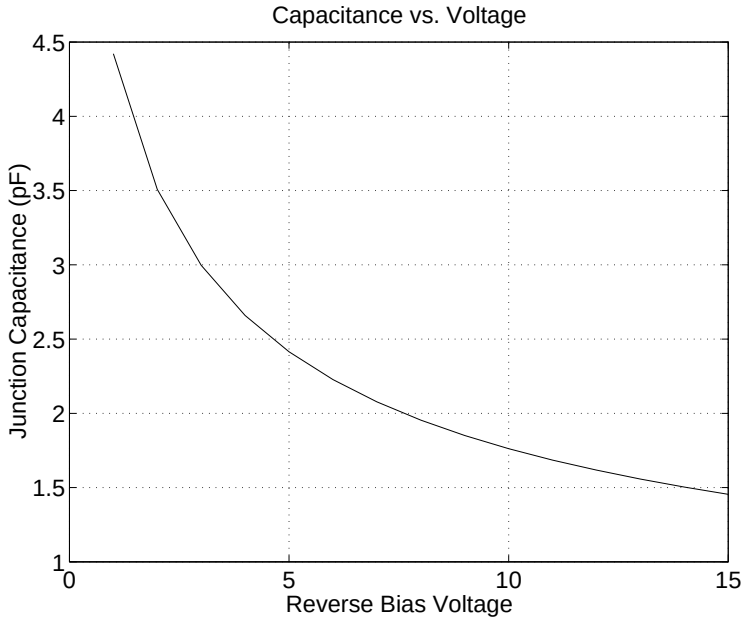


Figure 4.8: Capacitance vs. reverse bias voltage for the Toshiba 1SV280 varactor.

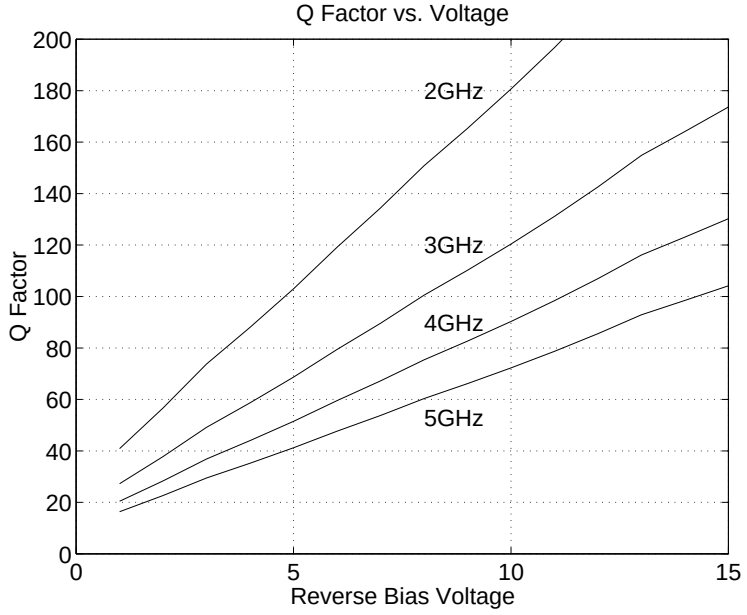


Figure 4.9. Q factor vs. reverse bias voltage for the Toshiba 1SV280 varactor at 2GHz, 3GHz, 4GHz and 5GHz.

4.5 Resonator with Varactor Tuning

The desired frequency tuning range of the oscillator developed here is between 2.5GHz and 5GHz. The capacitance tuning range of the 1SV280 is 3.04:1 with a minimum capacitance of 1.45pF and maximum capacitance of 4.42pF. The inductance is chosen by $L = \frac{1}{C(\omega_0)^2}$ where ω_0 is the resonant frequency. An inductance of 0.92nH will provide a 2.5GHz to 4.36GHz tunable resonance over 1V to 15V reverse bias. Although this is not a full octave of frequency tuning, the high Q of this varactor is considered more important than wide tuning range. Two oscillators may be used to tune over a more than an octave.

The inductance can be created using a very short length of microstrip line. A microstrip line has a relatively constant Q factor defined by Eq. 4.18 [13]. As the frequency increases, ωL increases, as does the resistance, R due to the skin effect of the line. The Q factor of a microstrip line with $\epsilon_r = 3.4$ is approximately 75 to 100 depending on the metal and dielectric losses. Denlinger measured a Q factor of 200 for a 50Ω microstrip resonator on alumina with an $\epsilon_r = 9.9$ at 4GHz in [29]. Simulations and measurements verify that a Q factor of 75 to 100 for a microstrip line on a lower dielectric constant with slightly higher losses is reasonable.

$$Q = \frac{2\pi f L}{R} = \frac{\beta}{2\alpha} \tag{4.18}$$

The worst case Q factor of the varactor is at low reverse bias voltages where the capacitance and resistance is highest. Assuming the Q of a microstrip line is about 80 and the Q of the varactor is 40 at 2GHz and 1V reverse bias, the Q of the resonator is calculated to be 26. Again assuming the microstrip line has a Q of about 80 with the Q of the varactor 130 at 4GHz and a reverse bias of 15V, the Q of the resonator is calculated to be 48.

A 0.92nH inductor is quite small so a modification is made to the resonator. Two diodes in series offer the same ratio of capacitance change and Q factor but have

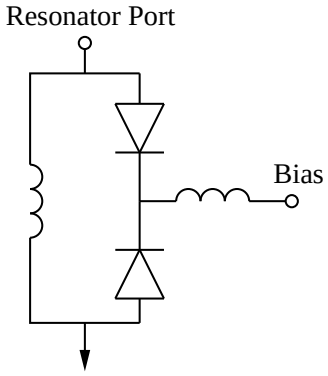


Figure 4.10: Shunt LC resonator with anti-parallel varactor diode tuning.

half the capacitance than a single diode. The inductance may then be doubled to 1.84nH to make fabrication easier. If the diodes are mounted in series with opposite polarity, called an anti-parallel configuration, the capacitance changes due to the large signal RF voltage present at the terminals is cancelled. While one varactor increases capacitance the other is reduced by the same amount assuming the capacitance to voltage curve can be approximated as linear. The antiparallel configuration can be seen graphically in Fig. 4.10. AM to PM conversion is the mechanism where amplitude changes within the oscillator are converted to frequency deviations. AM to PM conversion occurs when the large signal RF causes a capacitance change in the varactors and is turned into frequency deviation by $\omega_0 = \frac{1}{\sqrt{LC}}$. The small frequency deviation is measured as phase noise of the oscillator. The anti-parallel configuration cancels this effect.

4.6 Resonator Measurement

The resonator of Fig. 4.10 was constructed on 30mils thickness Rogers 4350 substrate. The diodes were spaced in series as close as possible with a microstrip inductor of 0.3mm thickness in parallel the length of the diodes.. The 50Ω tranmission line was connected at one terminal of the resonator and the other terminal grounded with a single 20mil via. There were a limited number of 1SV280 varactor diodes

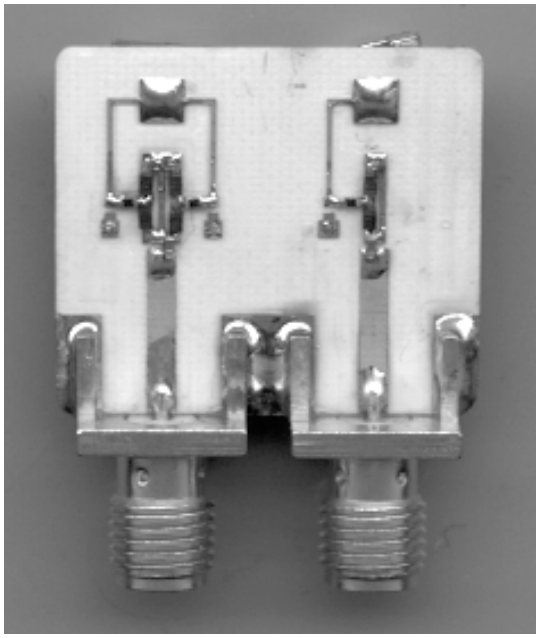


Figure 4.11. Photograph of the measured 2 varactor and 4 varactor resonator using Toshiba 1SV285 varactor diodes.

available and so a 1SV285 diode was used for this measurement. The 1SV285 has the same capacitance to voltage curve up to 10V as the 1SV280 but with slightly lower resistance. A photo of the measured 2-varactor resonator is shown on the right hand side in Fig. 4.11. A 4 varactor resonator (left side) was also measured but not used due to the higher capacitance and lower resonant frequency.

The S-parameters were measured from 500MHz to 6GHz for bias levels of 1V to 10V. Figure 4.12 shows the center frequency of oscillation vs. reverse bias voltage on the varactors. The resonant frequency ranged between 1.9GHz and 3.6GHz and is slightly lower than expected. The difference is due to the via ground inductance and package parasitics.

The measured reflection coefficients were converted to Zparameters and are plotted in Fig. 4.13. This plot shows the unloaded input impedance of the resonator. The unloaded Q factors ranged from 25 to 50 for biases of 1V to 10V respectively and are plotted in Fig. 4.15. This is very close to the calculated unloaded Q's of 26

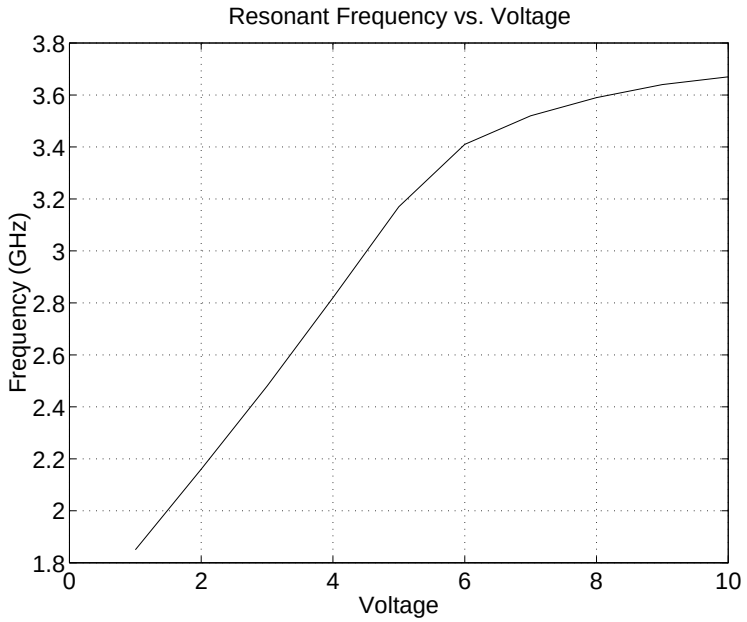


Figure 4.12: Resonant frequency vs. voltage change.

and 48 at 2GHz and 4GHz, respectively. The amplifier will load this resonator and effectively lower this Q. The optimum loaded Q of half the unloaded Q is achieved when the resonator is loaded with a 200Ω impedance. This was done graphically by caculating the Q from the BW of the Zin impedance of the resonator using $Q = \frac{f_0}{BW}$ while varying the load resistance R_{load}. The real input impedance for the loaded resonator is shown in Fig. 4.14. The comparison of Q factors between loaded and unloaded states assuming a loading of 200Ωs is shown in 4.15.

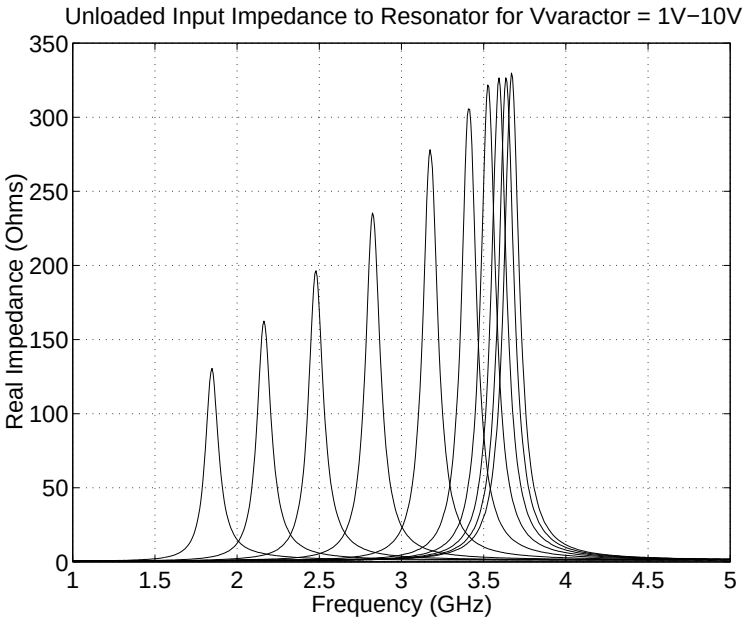


Figure 4.13: Input impedance of the 2 varactor resonator.

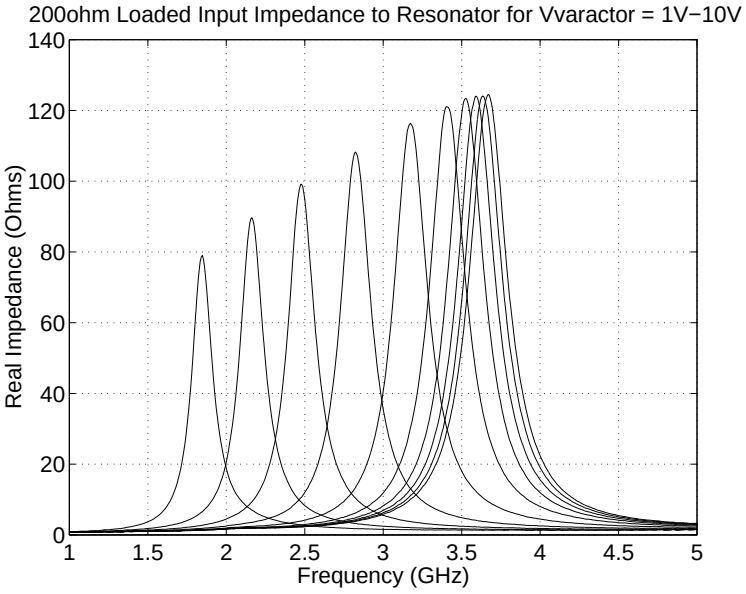


Figure 4.14: Input impedance of the 2 varactor resonator loaded with 200Ωs.

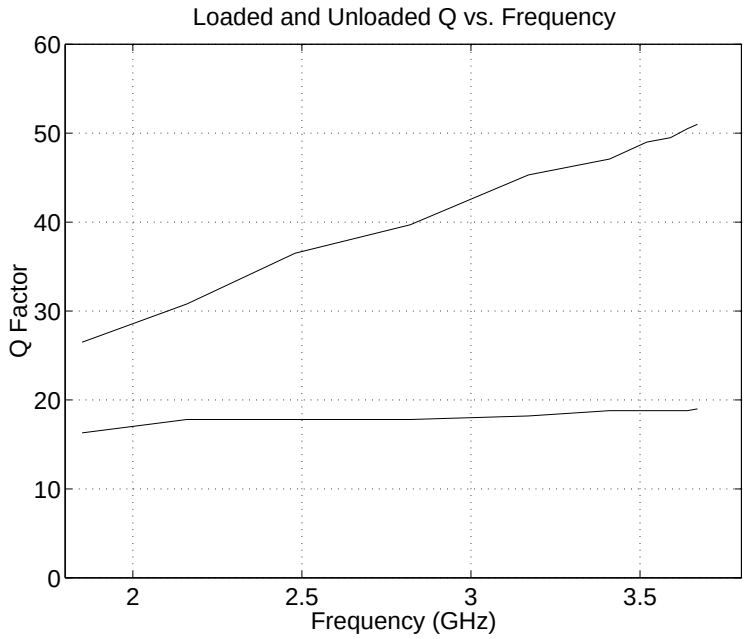


Figure 4.15. Q factor of resonator in unloaded and 200Ω loaded conditions vs. frequency.

CHAPTER 5

OSCILLATOR SIMULATION AND MEASUREMENT

5.1 Biasing the Oscillator

Before discussing the simulation methodologies, it is important to explain biasing of the oscillator as it directly affects the simulation. Biasing can have a negative effect on the overall performance if implemented poorly.

Three terminals on an oscillator need to be biased, two terminals on the transistor and one on the varactor, the remaining two are grounded. This is indepedent of configuration. In this design, it was chosen to bias the collector and base of the transistor because the emitter is easily grounded through the resonator inductor. The cathode of the varactor is biased to a positive voltage while the anode is grounded through the resonator. This creates the reverse bias for the varactors with a positive voltage.

The collector to emitter, V_{CE}, voltage must remain at the proper level for the desired frequency. The relevance of this can be seen in the measurements of the oscillator. In RF applications, the collector is generally biased using an inductor with a self resonance frequency as high as possible above the oscillation frequency. This ensures that it will not have an effect on the fundamental frequency of oscillation. The value of the inductor must be high enough to look like an RF open circuit. In a practical case such as this, two inductors are mounted in series: a 12nH inductor with self resonance frequency of 6GHz and a 100uH with a lower self resonance frequency. This creates a broadband RF open circuit. This is similar to the use multiple valued

capacitors in parallel to create a braodband RF short circuit. A resistor may be used to bias the collector but may unnecessarily load the output of the oscillator, lower the gain and degrade the phase noise.

The base terminal supplies the required I_C current by the relation $I_C = \beta I_B$. Textbooks typically show a voltage or current divider technique using resistors. This is fine for amplifiers but may contribute to the noise of the oscillator. Recall the noise due to a resistor is $V_n(f) = \sqrt{4kTR}$. In chapter 3 it is discussed that the noise due to the transistor may be modeled as a small resistance in series with the transistor. A small value for this resistor is desireable for low noise operation. Biasing with resistors effectively increases this noise which may be upconverted onto the fundamental frequency of oscillation as additional phase noise. Therefore, inductive biasing is generally preferred in high quality oscillator design. In this common base oscillator, the base inductance to provide negative resistance is RF shorted to ground by a 200pF capacitor and then a series combination of 12nH and 100uH are used to bias this point.

The last bias point is for the varactor(s). A varactor diode exhibits a capacitance to voltage change for reverse bias voltages. For a positive voltage bias, the diodes are mounted with the cathode grounded. Inductive biasing the varactors is crucial for good phase noise performance. In literature, it is common to show the varactors biased by a 10kΩ or 22kΩ resistor. A resistor provides an easy, resonant free way to bias the varactors. However, the large resistor voltage noise present at the terminals of the varactor will be upconverted as phase noise by the integration gain K(MHz/V) of the oscillator. The larger the integration gain, the more phase noise is present due to this resistance. The phase noise equation was modified by Rohde to show this AM to PM conversion in [30]. It is important to use only inductors and not capacitors to bias the varactors. A capacitor of significant value may introduce an extra pole in the feedback transfer function of a phase locked loop making it

unstable by reducing the phase margin.

It is worthwhile to discuss the reason behind using such large values of inductors and capacitors. Oscillators are highly sensitive to voltage fluctuations and upconvert any noise on the bias points listed above. While lab bench power supplies are quite good about regulating the large signal voltage, they are still quite noisy and may pick up additional noise in the cables running to the oscillator. Therefore a π-network is constructed before the 12nH inductor to reduce the noise. It consists of a 1uF capacitor to ground on each side of a 100uH series inductor. This network drastically attenuates any noise down to a few kHz. Larger values can be added to provide even more suppression.

5.2 Calculation and Simulation

Three methods were used to predict oscillator performance. Each method has it's own attributes which help in the design and analysis of a low phase noise oscillator. The first is using the two port analysis of a negative resistance oscillator. The second is analyzing a common base oscillator as a common base amplifier and one port resonator. The third analysis is a full nonlinear simulation using Agilent Technologies microwave simulation tool, Advanced Design System (ADS).

Redrawing a negative resistance oscillator as a 2-port network allows the amplifier and resonator to be analyzed separately. Figure 5.1 is a common base oscillator that has been redrawn using a virtual ground at the base. The BJT has been substituted for its small signal model. Here it can be seen that the R_{load} has a direct affect on the loading of the resonator. For the best phase noise $R_e||\frac{1}{g_m} + R_{load}$ should be set to the optimum value so the loaded Q is half the unloaded Q.

The second method treats the oscillator as a 1-port device. A common base amplifier with an inductance in the base will look like a negative resistance into the emitter terminal. Measuring the amplifier in this configuration and comparing

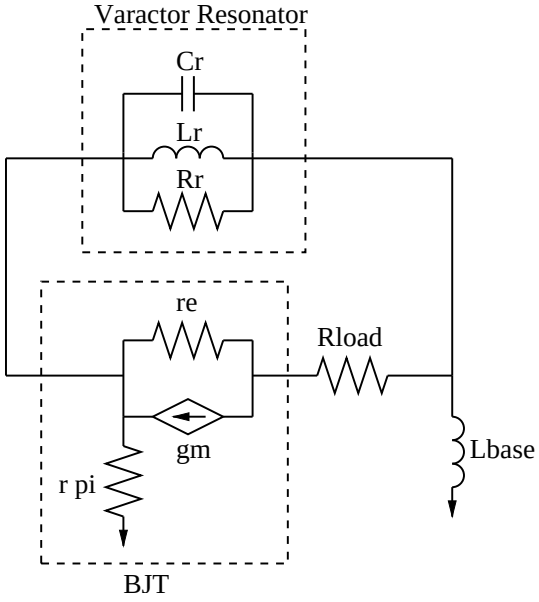


Figure 5.1. Common base oscillator redrawn using a virtual ground and a BJT small signal model.

the S_{11} and S_{21} curves for different values of inductance allow selection for the best broadband negative resistance in the desired frequency range. This measurement was done in chapter 3 for S_{11} in Fig. 3.9 and S_{21} in Fig. 3.10. The loaded resonator impedance can be seen in chapter 4 in Fig. 4.14. Figure 4.14 also shows how the oscillation frequency will change with varactor voltage.

The third method is a nonlinear simulation using Agilent Technologies Advanced Design System (ADS). ADS is capable of a harmonic balance simulation on an oscillator as well as a SPICE-like transient analysis. ADS accepts a full nonlinear model of the transistor and varactor. To validate the simulation models, a comparison was made between the nonlinear models for the hbfp-0420 and 1SV280 and measurements. There was good agreement to 6GHz.

The ADS schematic was drawn as closely to the actual circuit as possible including ground inductance from vias, microstrip lines used for inductors and small microstrip lines between elements. Figure 5.2 shows the schematic of the hardware

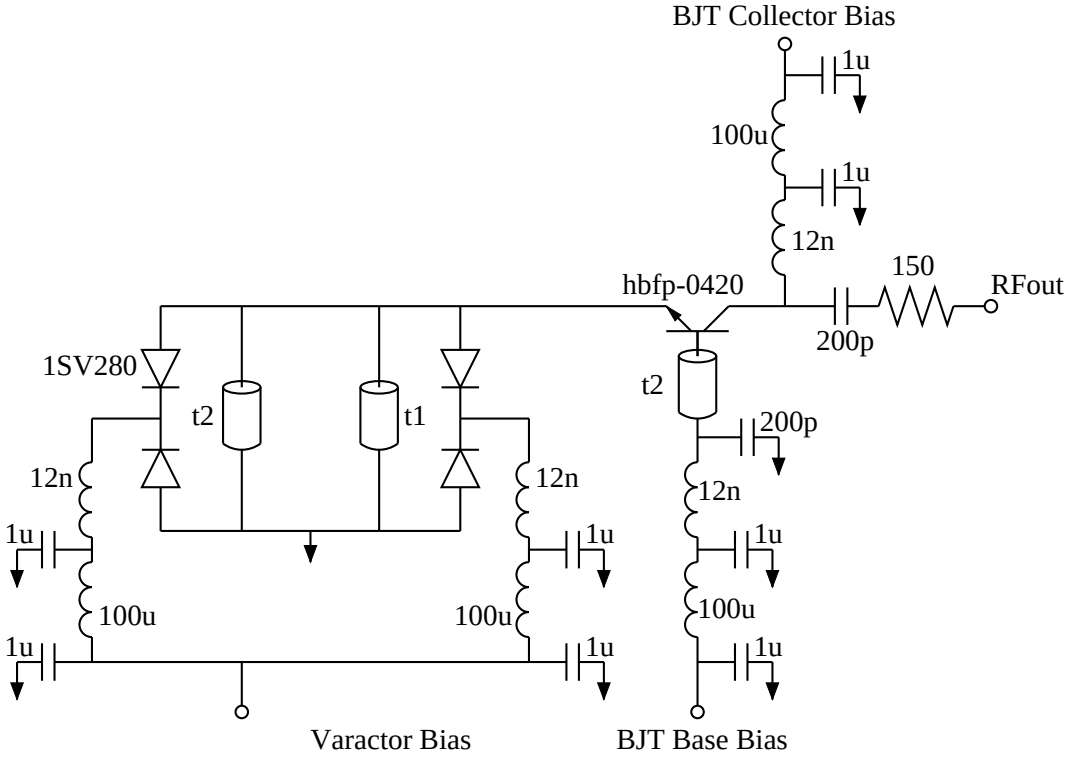


Figure 5.2: Schematic of the fabricated common base oscillator.

that the nonlinear simulation is based on. The analysis was done using the harmonic balance simulation method. ADS was setup to calculate power output of the fundamental frequency up to the 4th harmonic, phase noise and DC currents and voltages.

The initial ADS simulation was carried out to predict the performance of a fabricated oscillator. The resonator values and length of line between the oscillator and resonator was adjusted for oscillation to occur from 1V to 15V on the varactor. The initial design swept from 2.5GHz at 1V to 5GHz at 15V. The phase noise ranged from -85dBc(f_m=10kHz) at 1V(2.5GHz) to -90dBc(f_m=10kHz) at 15v (5GHz). However, pad capacitance and an accidental misfabrication of the microstrip inductor to 0.3mm thickness instead of 0.5mm led to a frequency tuning range of 1.9GHz to 3.8GHz. The values in the simulation were adjusted to match the physical dimensions of the fabricated part and the resulting simulation vs. measured figures

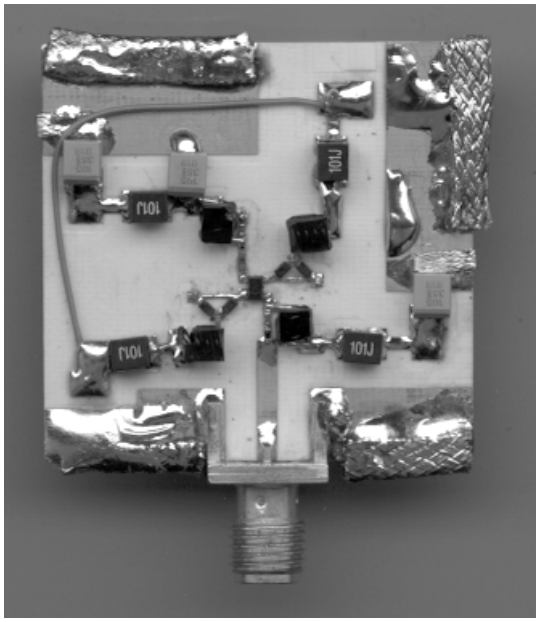


Figure 5.3. Photograph of the measured 1.9GHz to 3.8GHz varactor tuned oscillator.

use this data.

5.3 Measurements

The common base oscillator was made on a 30mils thickness Rogers 4350 substrate. The resonator is a 2mm x 0.3mm section of microstrip line. Pads for devices were of minimum size. The 200pF capacitors are of 0402 size to reduce any lead inductance. The 12nH inductors are a Coilcraft component and are air-core. The 100uH inductors are from Toko. The RFout line was mated to a board launch SMA connector and the three DC bias points used SMB connectors. A photo of the measured oscillator is shown in Fig. 5.3.

Measurements were made using 3 Hewlett-Packard digital DC supplies and a Hewlett-Packard 8562B 22GHz Spectrum Analyzer. The frequency vs. voltage measurements and power levels were made using the 3MHz resolution bandwidth. The phase noise was measured using a 1kHz bandwidth and a span of 1Mhz centered on the oscillation frequency. A single sweep measurement was made and the phase

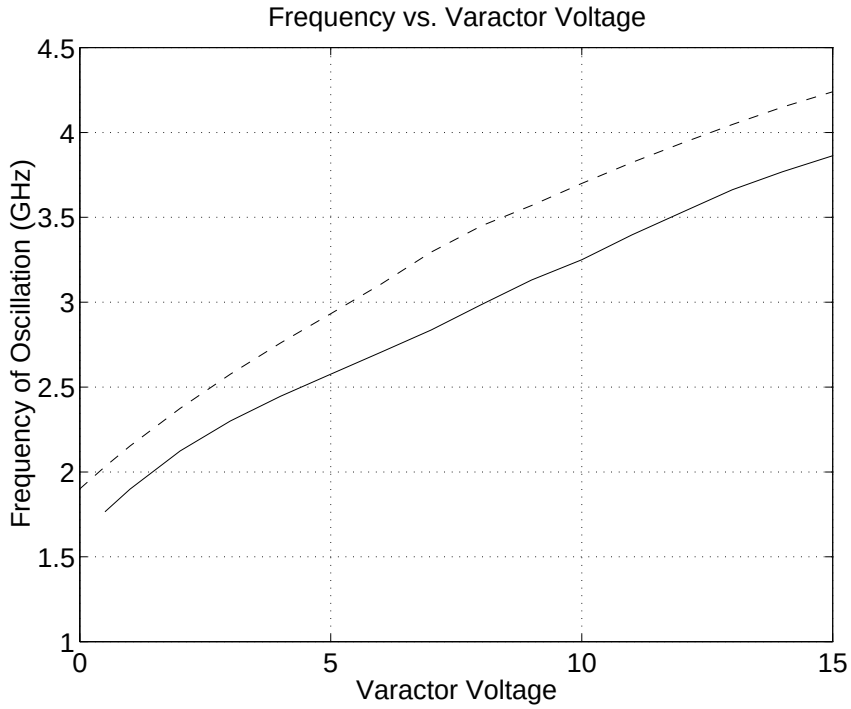


Figure 5.4. Oscillation frequency vs. varactor voltage of measured (solid) vs. simulated (dashed) oscillator.

noise was measured using the delta function of the cursors at 100kHz offset. The measured values were renormalized to a 1Hz bandwidth by subtracting 30dB from the measurements ($10\log(1kHz)$).

Figure 5.4 shows the frequency of oscillation vs. varactor voltage for the measured (solid line) and simulated (dashed line) data. Both curves show an integration constant of $K = 135\frac{MHz}{V}$. The frequency to voltage relationship is close to linear, therefore external linearization circuitry is not required. An abrupt varactor with higher breakdown voltage may be used here to reduce the integration constant K.

A phenomenon known as f/2 was measured in the oscillator at frequencies under 3GHz and at high V_{CE} voltages. This is a subharmonic that develops at exactly half the fundamental frequency of oscillation with approximately 20dB lower power. The mixing products at $\frac{3}{2}f_0$ and at multiples of $n\frac{1}{2}f_0$ are also seen. The

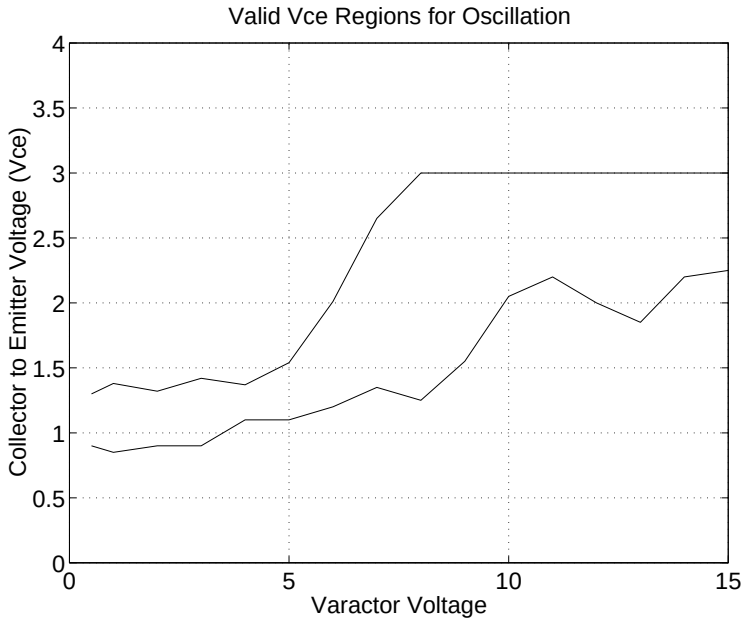


Figure 5.5. Valid regions of oscillation for V_{CE}. Above this V_{CE} level the oscillator exhibited an f/2 subharmonic. The lower limit is -10dBm.

f/2 occurs when the V_{CE} is above some threshold. The regions for valid oscillation are shown in Fig. 5.5. The upper limit was determined by the maximum V_{CE} value to which the f/2 is not produced. The lower limit was determined by the point at which the power is -10dBm. Below that power level the oscillator is not much use, although it will oscillate.

Two experiments were done in an effort to isolate the cause of the f/2. First, a coupler was put in front of the resonator to measure reflected power in a large signal condition. A frequency source supplied +15dBm of power at frequencies between 2GHz and 4GHz and the output was observed with a spectrum analyzer. The f/2 was not be reproduced.

The second experiment involved driving the amplifier into very heavy saturation with a frequency source. The power input was varied up to +10dBm at frequencies between 2GHz and 4GHz while the output was monitored with a spectrum analyzer. Again the f/2 was not reproduced.

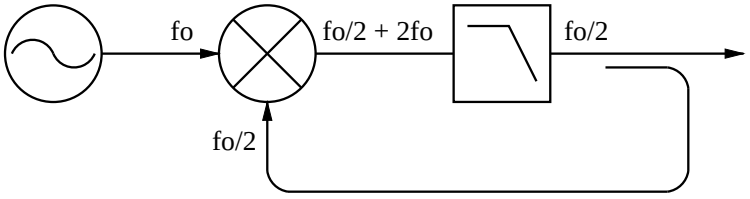


Figure 5.6: Block diagram of an analog frequency divider.

One possibility is that the amplifier is acting as an analog frequency divider at lower frequencies. Figure 5.6 shows the block diagram of an analog frequency divider using a mixer [31]. The pn junctions within the BJT may be acting like the nonlinear mixer shown causing a sustained f/2 at lower V_{CE} voltages.

The output power was measured for the maximum V_{CE} voltage without producing an f/2. The simulation did not show the f/2 so in a fair comparison the V_{CE} value for simulation was adjusted to the same level used for the measurement. Figure 5.7 is a plot of the output power vs. varactor voltage for the measured (solid) vs. simulated (dashed) data. There is only a 2dB difference in output power vs. measured power. The simulation also predicts the reduced output power due to the lowered V_{CE} voltage. Finding the cause of the f/2 will allow the V_{CE} voltage to be raised, increasing the power output in the lower half of the frequency range.

The most important parameter of this oscillator is phase noise. The measured (solid) vs. simulated (dashed) phase noise is shown in Fig. 5.8. The phase noise was measured on a spectrum analyzer at 100kHz offset using a 1kHz BW and renormalized by adding $10\log(1kHz)$ to the measured data. The oscillator was free running and so measurements at 10kHz offset were too difficult. The phase noise was measured and simulated at the maximum permissible V_{CE} voltage. The original simulation, before being adjusted to match fabrication, did not show the rise in phase noise midband seen in Fig. 5.8. The bottom curve (dashed) is the predicted phase noise given that the loaded Q is exactly half the unloaded Q of the resonator from Fig. 4.15. This was calculated by the use of Eq. 2.16 assuming $P_o = 0dBm$,

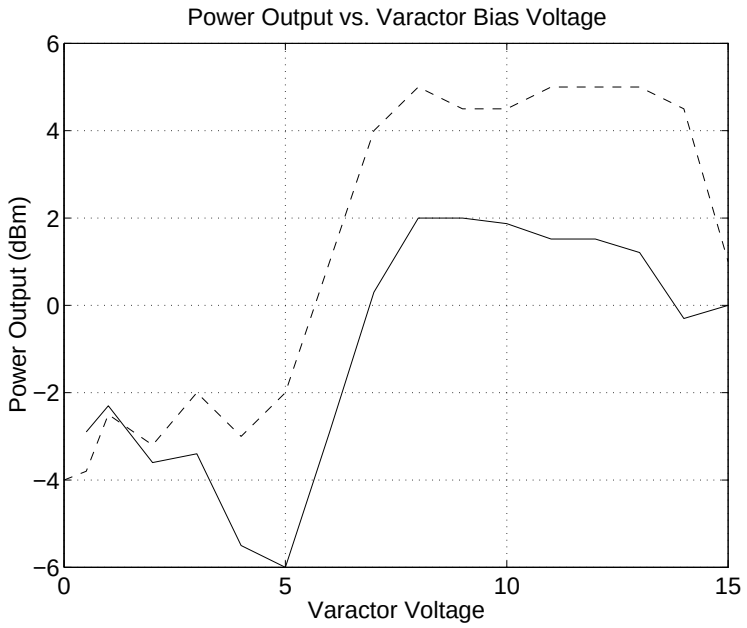


Figure 5.7. Power output vs. varactor voltage of measured (solid) vs. simulated (dashed) oscillator.

$F = 6dB$ and $f_c = 1kHz$. The added phase noise may be due to the $n2\pi$ phase shift not being centered in the resonators passband, thereby the loaded Q of the oscillator. A more controlled fabrication as well as building several units with slightly different values of inductances and spacing between the resonator and amplifier would fine tune this oscillator design.

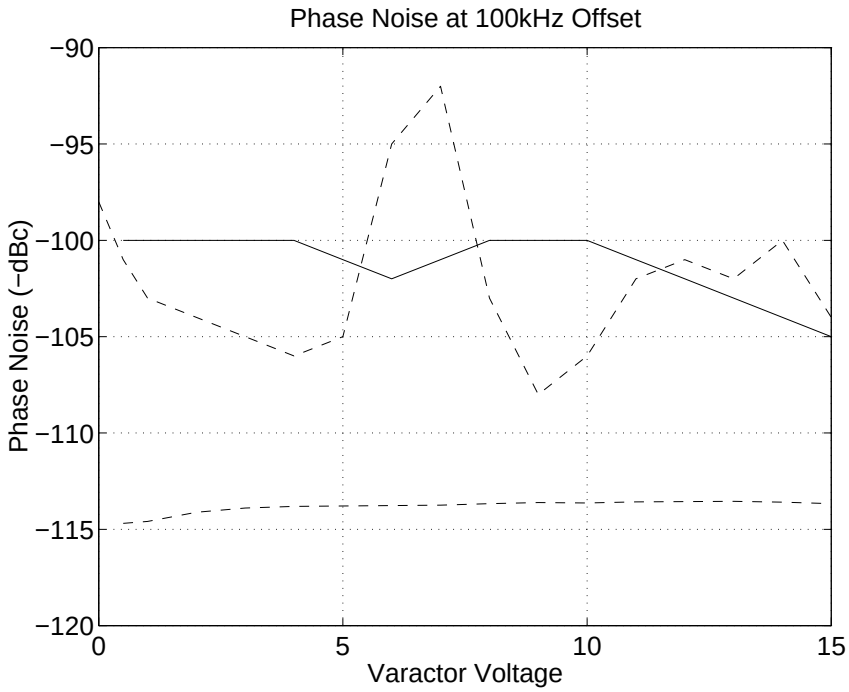


Figure 5.8: Phase noise at 100kHz offset for measured, simulated and theoretical

CHAPTER 6

OSCILLATOR IMPLEMENTATION IN A PHASE LOCKED LOOP

6.1 Phase-Locked-Loop Theory

A phase-locked-loop (PLL) is a system in which a higher frequency oscillator is 'locked' to a very stable, lower frequency oscillator. The motivation behind this lies in the difficulty of designing both a wide band and ultra stable oscillator. The two design goals are contradictory. A phase locked loop compares the close in phase noise of a tuneable oscillator (high frequency) with that of a stable reference such as an oven-controlled crystal oscillator. The phase difference is sent as feedback to the varactor controlled oscillator (VCO) and the phase noise of the VCO is reduced to the level of the lower frequency oscillator. Figure 6.1 is the schematic of the PLL built to phase-lock the oscillator designed here.

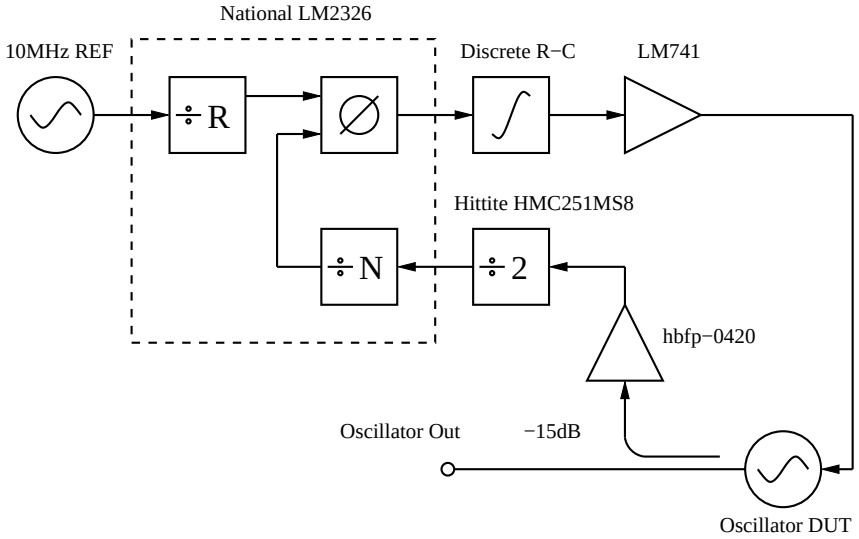


Figure 6.1: Phase-lock loop schematic for 3GHz to 6.0GHz operation.

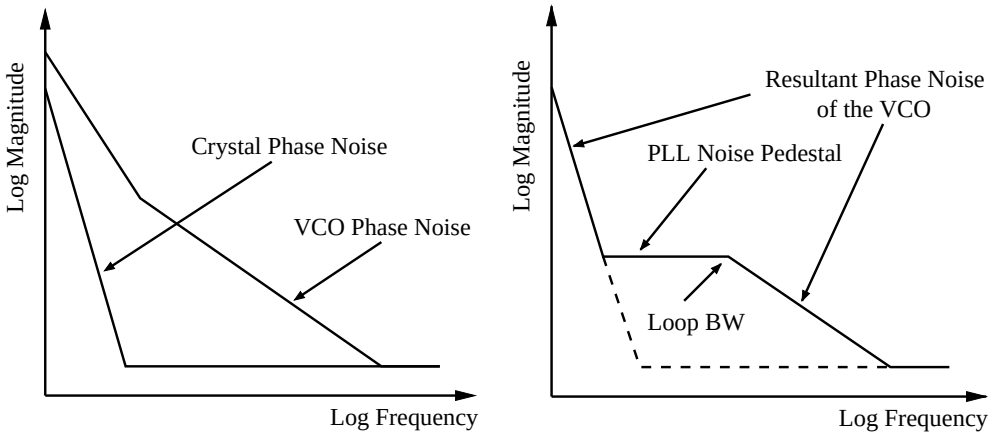


Figure 6.2. Qualitative phase noise comparison between a crystal reference and VCO in 6.2(a). The resultant phase noise of the VCO phase locked to the crystal oscillator in 6.2(b)

This PLL is called an integer-N system. This means the VCO frequency and the crystal reference are some integer multiple of the reference frequency. The two sinusoids are put through a limiter and compared digitally using a digital phase detector. The phase difference is measured in pulses that control a charge pump circuit. The latter raises or lowers the varactor voltage of the VCO to keep the oscillators in phase-lock.

The disadvantage of this system is twofold. First, the phase noise is only improved within the bandwidth of the loop response. Second, there is a noise pedestal from the frequency division of the signal that is an absolute limit of the phase noise improvement. Figure 6.2(a) shows the qualitative difference in phase noise between a 10MHz crystal reference oscillator and a VCO. Figure 6.2(b) demonstrates graphically the phase noise improvement, loop bandwidth and divider noise pedestal. The noise pedestal is determined by Eq. 6.1 [32]. N_{floor} is a measured quantity from the device itself, usually due to the process. The value given for this PLL is -206dB. The quantitiy $10\log(f_{reference})$ is due to the phase detector. The term $20\log(N)$ is

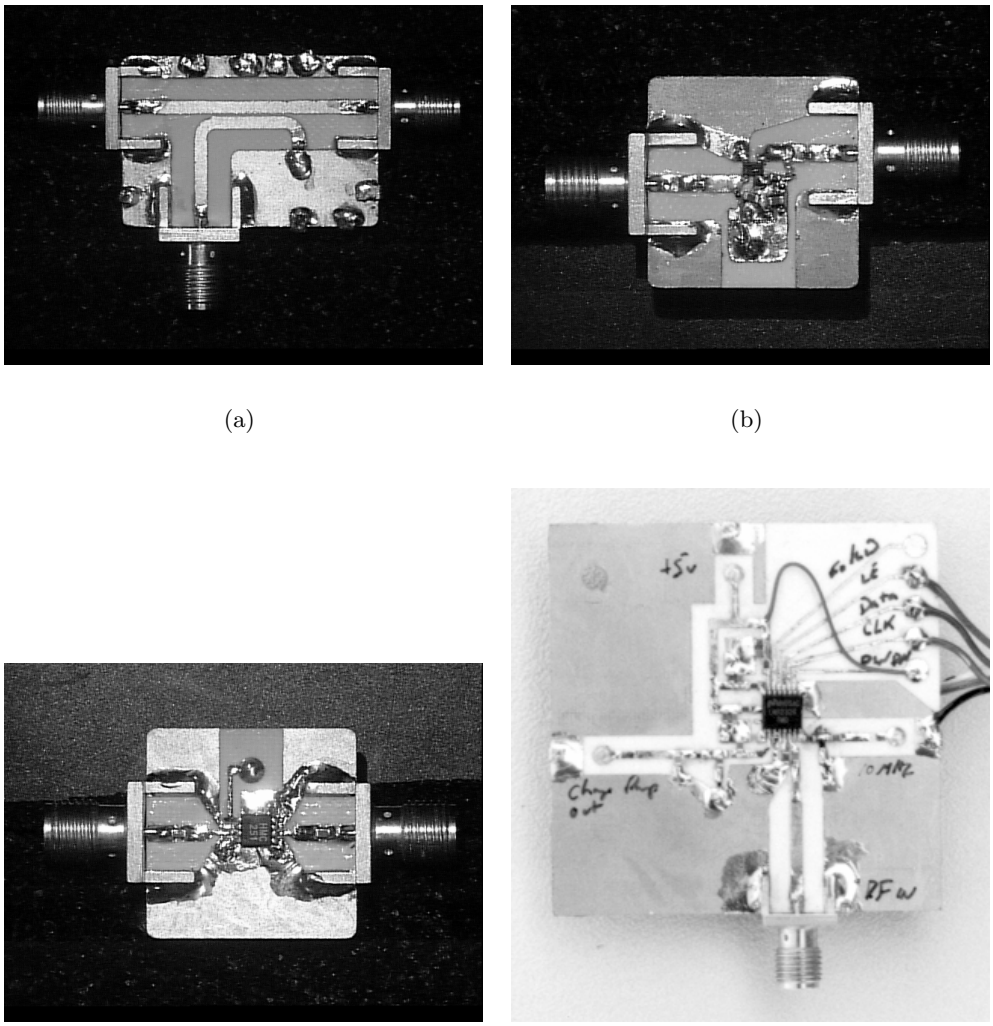
noise due to dividing the signal.

$$Pedestal(dBc/Hz) = N_{floor} + 10\log(f_{reference}) + 20\log(N) \tag{6.1}$$

6.2 Hardware Measurements

The hardware was constructed from commercially available components. The phase locked loop is a National Semiconductor 2326 component, capable of phase locking a VCO between 500MHz and 3GHz. The charge pump filter is a 3-pole designed using software from National Semiconductor. To extend the frequency range, a 3GHz to 6.5GHz divide-by-two prescaler was used from Hittite. An additional hbfp-0420 amplifier was used to to set the correct power level for proper operation of the Hittie prescaler. The coupler is a simple -15dB microstrip coupler designed to work from 2.5GHz to 5GHz. Photos of the components used in the system are shown in Fig. 6.3. The complete system, including VCO, is shown in 6.4. Batteries were used to power the system to eliminate any power supply noise. Four 9-volt batteries were used to supply +27V and -9V.

The PLL was programmed via a laptop computer and parallel port cable. Frequency changes were done using software provided by National Semiconductor. The loop filter for the charge pump was set to be a very narrow 1kHz so the phase noise of the free running oscillator could be measured at 10kHz. Unfortunately the BW available on the spectrum analyzer was not small enough to measure phase noise at less than 100kHz offset.



(a) (b)

(c) (d)

Figure 6.3. Photographs of components used to build the phase-locked loop. The microstrip coupler is shown in 6.3(a), the Agilent Technologies hbfp-0420 amplifier in 6.3(b), the Hittite prescaler in 6.3(c) and the National Semiconductor PLL in 6.3(d).

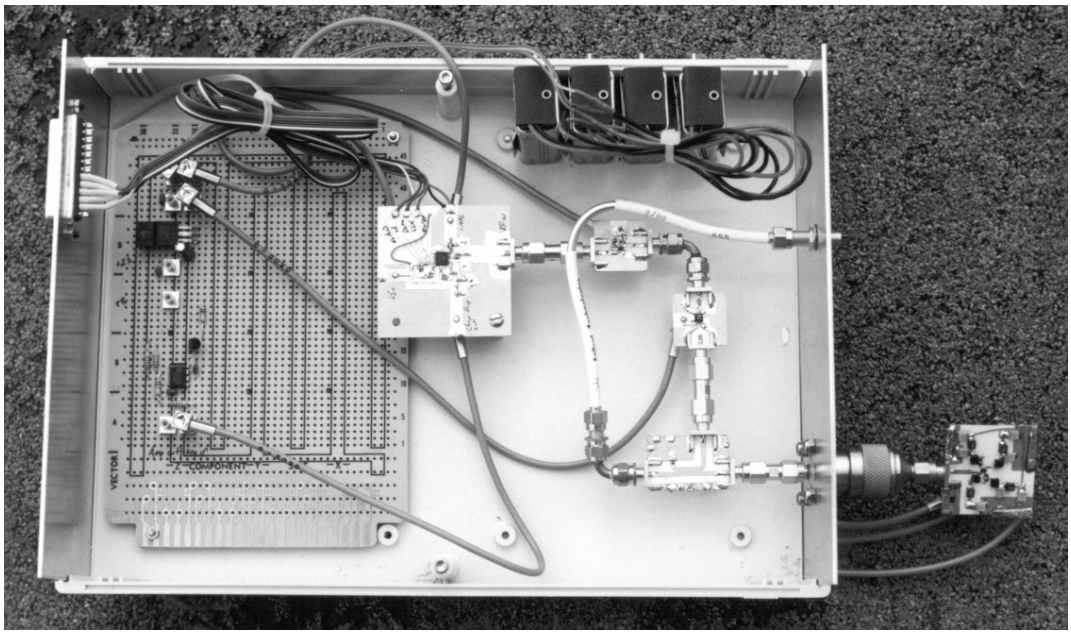


Figure 6.4: Photo of assembled phase locked loop system with VCO.

CHAPTER 7

FUTURE WORK AND CONCLUSIONS

7.1 Future Work

Current theory predicts that a 2.5GHz to 5GHz oscillator may have a phase noise at 10kHz offset of -93dBc. This is still approximately 7dB to 12dB worse than current YIG tuned oscillators. A phase-locked-loop is capable of improving the phase noise inside the locking bandwidth, usually from a few kHz out to 1MHz, but not more than the noise pedestal of the phase lock loop. The current state of the art in phase-locked-loops is a divider pedestal about -100dBc to -110dBc. This is using fractional-N technology. A proposed improvement involves the use of a frequency discriminator. A frequency discriminator is commonly used to measure phase noise of an oscillator [14] or in a feedback configuration to improve it [33] [34] [35].

A frequency discriminator, shown in Fig. 7.1, uses a phase detector to compare the output of an oscillator with an output from the oscillator that is delayed in time by τ_d. The difference in phase between the delayed and undelayed signal is measured as phase noise. The delayed and undelayed signals must be in exact quadriture with each other for maximum sensitivity. Negative feedback from a quadriture sensor controls a variable phase shifter. The signals are in quadriture when the DC voltage of the mixer is zero. The phase noise spectrum is translated to baseband and is referred to 0Hz instead of f_0. This is low pass filtered and sampled digitally with an FFT analyzer after a low noise amplifier (LNA).

The sensitivity is determined by the transfer function of the system shown

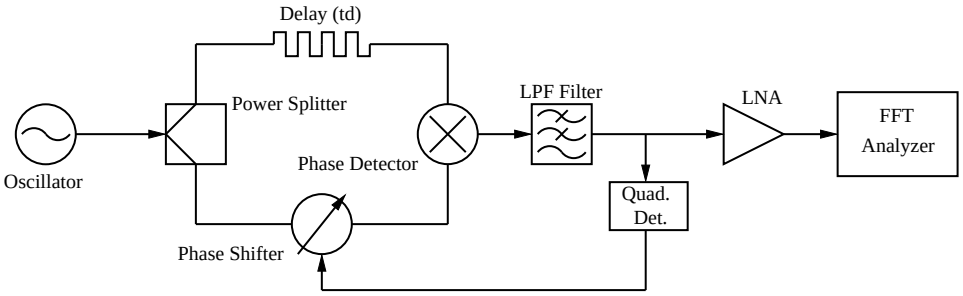


Figure 7.1: Frequency discriminator used to measure phase noise.

in Eq. 7.1. The output voltage fluctuation $\Delta V(f_m)$ are proportional to the frequency fluctuations $\Delta f(f_m)$. Sensitivity is set by the delay τ_d and phase detector constant K_ϕ. The transfer function has a $\frac{sin(x)}{x}$ response as shown in Fig. 7.2. A large delay will have better sensitivity closer in to the carrier but the null will limit the BW. A shorter delay will produce less sensitivity but allow an improvement farther out in the spectrum.

$$\Delta V(f_m) = \left[K_\phi 2\pi\tau_d \frac{sin(\pi f_m \tau_d)}{(\pi f_m \tau_d)} \right] \Delta f(f_m) \tag{7.1}$$

This system may be used as in a feedback loop much the same way as a phase-locked-loop system. Figure 7.3 depicts a possible implementation. The system offers best sensitivity at offset frequencies f_m less than $\frac{1}{2\pi\tau_d}$. Below this frequency

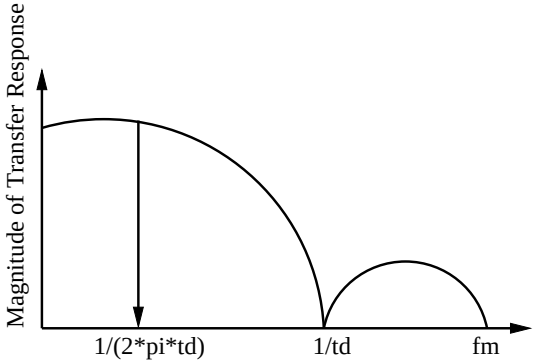


Figure 7.2. Transfer function of frequency discriminator showing sin(x)/x response and BW limit.

the $\frac{sin(x)}{x}$ response may be ignored and the transfer response written as Eq. 7.2.

$$\Delta V(f_m) = K_\phi \pi \tau_d \Delta f(f_m) \tag{7.2}$$

The sensitivity is proportional to the phase detector constant K_ϕ and length of delay τ_d. The phase detector is usually a low level microwave mixer. The level corresponds to the amount of LO drive is required to turn the mixer on. The optimum sensitivity is achieved when the undelayed signal is at the specified LO drive level and the delayed signal is 8.7dB below the phase detector's compression point [14].

The effective Q factor Q_E is related to the phase delay of a system by Eq. 7.3. Therefore the phase noise improvement can be determined by Eq. 2.16. The limit of improvement is reached when Q_E of the delay τ_d becomes equal to the Q factor of the transmission line used for the delay. To this extent the losses of the line become greater than the benefit received. A high quality buffer amplifier may be used along the delay τ_d if the noise figure and flicker noise are acceptable. This eliminates the need for a very high Q coaxial line or limited length.

$$Q_E = \pi f_0 \tau_d \tag{7.3}$$

$$\tau_d < \frac{1}{2\pi f_m} \tag{7.4}$$

There is a compromise between phase noise improvement and the bandwidth where this improvement occurs. Improving the phase noise by 12dB, reaching -105dBc at 10kHz offset for a VCO 5GHz, would require a line with Q_E of 125. This limits the delay to $\tau_d = 8nS$. This line will improve the phase noise up to 20MHz. A delay of 8nS is 2.4meters in an $\epsilon_r = 1$ or 0.8meters in microstrip with $\epsilon_r = 10$. The variable phase shifter used to keep the quadriture for the phase detector may be created from a capacitively loaded line using varactors.

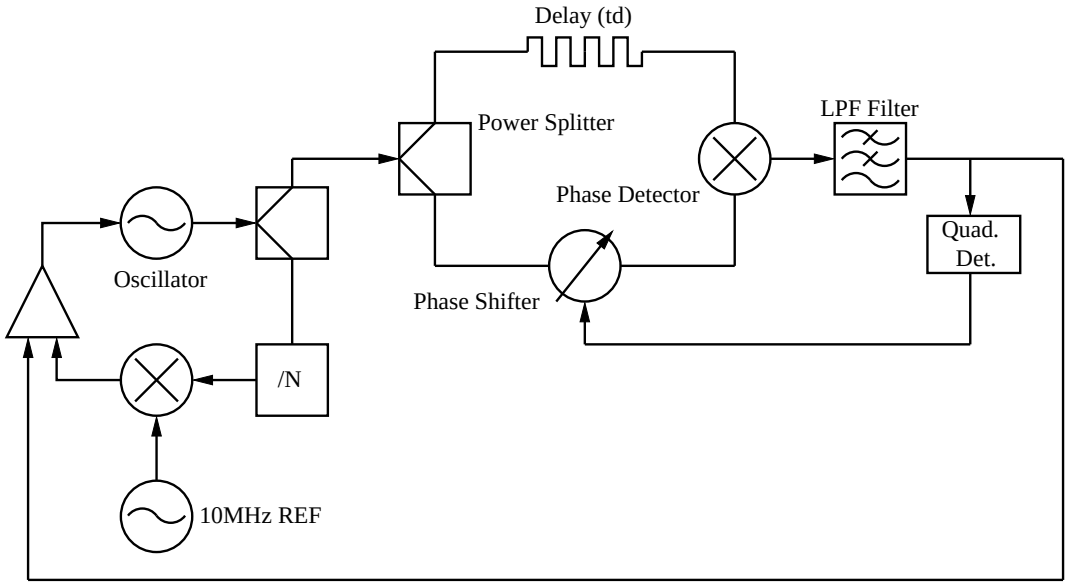


Figure 7.3. Frequency discriminator combined with phase locked loop to improve far out and close in phase noise, respectively.

7.2 Conclusions

The theory, simulation and design of a 1.9GHz to 3.8GHz varactor tuned oscillator has been presented. All previous octave tuning varactor oscillators known to the author have been below 3GHz. The octave tuning oscillator presented has a measured a phase noise of -85dBc 10kHz offset from the carrier at 3.8GHz and 3dBm output power. The theoretical limit is -93dBc and -90dBc was achieved in simulation with an octave of tuning from 2.5GHz to 5GHz. The theoretical phase noise for this varactor tuned oscillator is 12dB higher than a similar YIG oscillator but offers one order of magnitude faster tuning speed, lower current consumption and lower cost. This work presents a viable alternative to a YIG oscillator for microwave test instrumentation or other systems requiring octave tuning. Figure 7.4 is a phase noise comparison between current high performance, octave tuning varactor oscillators, a typical YIG oscillator and the measured, theoretical and future phase noise for the VCO presented here. The measured values have been extrapolated for frequencies less than 100kHz assuming an f_c of 8kHz, similar to the other oscillators shown.

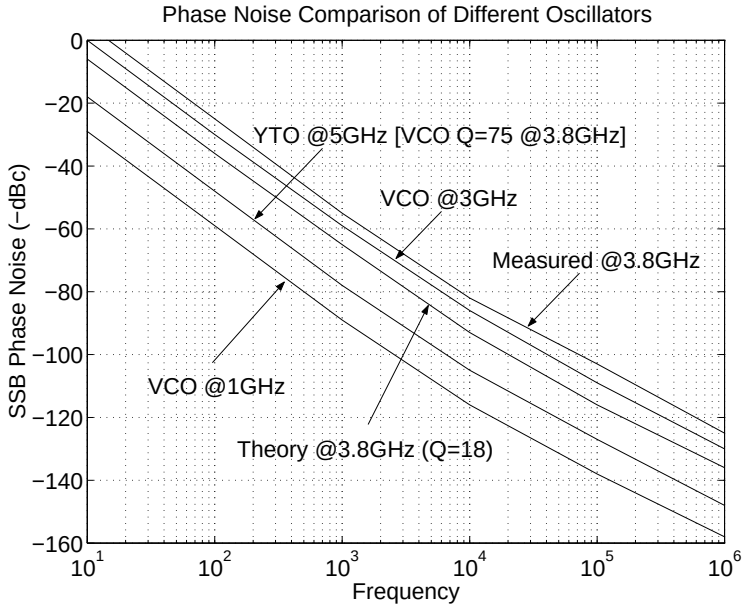


Figure 7.4. Phase noise comparison of different octave tuning oscillators including the measured VCO at 3.8GHz, the theoretical phase noise of this 3.8GHz oscillator and the theoretical phase noise of a 3.8GHz oscillator using a frequency discriminator.

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